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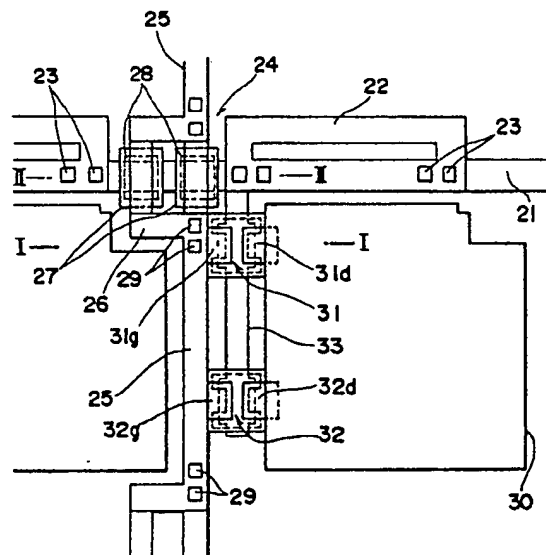
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(54) An active matrix substrate for liquid crystal display.

(57) An active matrix substrate for the liquid crystal display has a switching circuit for switching on each of picture elements which is comprised of the corresponding gate bus line, source bus line and a switching transistor and the switching circuit includes at least one redundant structure for avoiding the inoperativeness of the switching circuit.

Fig.1



An active matrix substrate for liquid crystal display

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an active matrix substrate for liquid crystal display on which a switching matrix with use of thin film transistors is formed to drive an individual picture element.

Description of the Prior Art

The liquid crystal display having picture elements arranged in a matrix form, as shown in Fig. 23 schematically, is widely used. Especially, the liquid crystal display panel is widely used for the display of an electronic apparatus such as a personal computer of lap-top type or the like.

In a recent liquid crystal display panel, so called active matrix substrate is used on which a number of thin film transistors are formed in a matrix form. As shown in Fig. 21 schematically, each thin film transistor (TFT) switches on the corresponding transparent electrode PE for a picture element when designated through both of gate and source bus lines GBL and SBL.

Fig. 23 shows a cross-sectional view along A-A line of Fig. 22.

An insulation film 1a is formed on a glass substrate 1 and, a gate electrode 3 is formed together with the gate bus line GBL on the insulation film 1a by etching Ta film.

This gate electrode 3 and the gate bus line GBL are covered with an anodic oxide film 4 of Ta_2O_5 and a gate insulator 5 of $SiNx$ is formed so as to cover whole of the former insulation film 2 including the anodic oxide film 4. On the area of the gate insulator 5 covering the anodic oxide film 4, a thin film transistor TFT is formed to switch on a transparent electrode 6 for each of picture elements formed on the gate insulator 5. The thin film transistor TFT is formed so as to have a drain electrode 7 connected with the picture element electrode 6, a source electrode 8 connected to the source bus line SBL, and a semiconductor film 9 of amorphous silicon (a-Si) formed above the gate electrode 3. This semiconductor film 9 is connected to the drain electrode 7 and the source electrode 8 through a film 10 of amorphous silicon and is covered by a protection film 11.

According to this structure, TFT is switched on by applying a predetermined voltage to the gate electrode 3 through the gate bus line GBL and,

therefore, a voltage applied to the source bus line SBL is applied to the picture element electrode 6 through the a-Si semiconductor film 9.

The gate bus line GBL and the source bus line SBL are insulated with each other at their crossing zone by an a-Si (i) / a-Si (n^+) layer 12 and covered by an etching stopping layer 13.

In such a structure of the active matrix substrate, if a gate bus line GBL or a source bus line SBL is broken, all of picture element electrodes aligned along the broken bus line becomes inactive to cause a line defect of an image to be displayed. Also, if a TFT is broken, the corresponding picture element is made inactive.

Conventionally, various efforts regarding the production process have been made in order to avoid these defects. However, it is impossible to avoid them completely only by improving the production process.

SUMMARY OF THE INVENTION

One of objects of the present invention is to provide a structure of the active matrix substrate for liquid crystal display which is capable of minimizing possible image defects such as line defect, picture element defect and the like.

Another object of the present invention is to provide a structure of the active matrix substrate which is capable of preventing possible line defects caused by bus line breaks.

A further object of the present invention is to provide a structure of the active matrix substrate which is capable of preventing possible picture element defects due to inoperative TFTs.

BRIEF DESCRIPTION OF DRAWINGS

These and other objects and features of the present invention will become more apparent when the preferred embodiment of the present invention is described in detail with reference of accompanied drawings in that:

Fig. 1 is an explanative enlarged plan view of a portion of the active matrix substrate according to the present invention;

Fig. 2 is an explanative enlarged plan view for showing the first step of the production process of the active matrix substrate;

Fig. 3 is a schematic cross-sectional view along III-III line of Fig. 2;

Fig. 4 is an explanative enlarged plan view for showing the second step of the production process;

Fig. 5 is a schematic cross-sectional view along IV-IV line of Fig. 4;

Fig. 6 is an explanative enlarged plan view for showing the third step of the production process;

Fig. 7 is a schematic cross-sectional view along V-V line of Fig. 6;

Fig. 8 is a schematic cross-sectional view along V-V line of Fig. 6 for showing the result obtained by performing the third step;

Fig. 9 is an explanative enlarged plan view for showing the fourth step of the production process;

Fig. 10 is a schematic cross-sectional view along VI-VI line of Fig. 9;

Fig. 11 is a schematic cross-sectional view along VI-VI line of Fig. 9 for showing the result obtained by performing the fourth step;

Fig. 12 is an explanative enlarged plan view for showing the fifth step of the production process;

Fig. 13 is a schematic cross-sectional view along VII-VII line of Fig. 12;

Fig. 14 is an explanative enlarged plan view for showing the sixth step of the production process;

Fig. 15 is a schematic cross-sectional view along VIII-VIII line of Fig. 14;

Fig. 16 is a schematic cross-sectional view along VIII-VIII line of Fig. 14 for showing the result obtained by performing the sixth step;

Fig. 17 is an explanative enlarged plan view for showing the seventh step of the production process;

Fig. 18 is a schematic cross-sectional view along line IX-IX of Fig. 17;

Fig. 19 is a schematic cross-sectional view along line IX-IX of Fig. 17 for showing the result obtained by performing the seventh process;

Fig. 20 is a schematic cross-sectional view along line II-II of Fig. 1;

Fig. 21 is a schematic plan view showing an active matrix substrate;

Fig. 22 is a schematic enlarged plan view showing a portion of a conventional active matrix substrate; and

Fig. 23 is a schematic cross-sectional view along line A-A of Fig. 22.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 shows an enlarged plan view of a portion of the active matrix substrate according to the

present invention.

As shown in Fig. 1, a gate bus line 21 and a source bus line 25 are formed so as to cross at right angle with each other. A transparent picture element electrode 30 is formed in each square area defined by adjacent two bus lines and adjacent two source bus lines. Each picture element electrode 30 is switched on or off to the source bus line 25 by two thin film transistors (TFTs) 31 and 32.

These two TFTs 31 and 32 are arranged parallel on a gate electrode 33 which is formed so as to extend parallel to the source bus line 25 on an area defined between the same and the picture element electrode 30.

In the present preferred embodiment, various redundant structures are provided for the gate bus line 21, the source bus line 25 and the switching structure of each picture element electrode 30.

With respect to the gate bus line 21, there is provided a bypass bus line 22 at every picture element electrode 30 which is elongated parallel to the gate bus line 21 and terminated before the crossing zone 24 with the source bus line 25.

Further, the part of the gate bus line 21 parallel to the bypass bus line 22 and the latter are made as a double layered structure, as will be explained later.

With respect to the source bus line 25, a bypass bus line 26 which bypasses the crossing portion thereof with the gate bus line 21 is formed at the crossing zone 24 and the remaining portion thereof except for the crossing zone is made as a double layered structure.

With respect to the switching structure for each picture element electrode 30, each gate electrode 33 is formed elongated parallel to both of the source bus line 25 and the side of the picture element electrode 30 and, two TFTs 31 and 32 are formed parallelly on the gate electrode 33, which are able to switch on or off the picture element electrode 30 to the source bus line 25, as mentioned above.

Hereinafter, these redundant structures will be explained more concretely together with the production process of the active matrix substrate.

[First step]

At first, a thin film of tantalum (Ta) with a thickness of 500 to 5,000 Å is deposited on a surface of an insulated glass substrate 50.

Then, as indicated as cross-hatched areas in Figs. 2 and 3, individual patterns corresponding to the gate bus line 21; the bypass bus line 22 thereof, the source bus line 25 and the gate electrode 33 are formed by photoetching the tantalum

film. The bypass bus line 22 is formed parallel to the gate bus line 21 and terminated before the crossing zone 24 in order not to increase possible leak and stray capacitance between two bus lines 21 and 25.

In this step, the pattern for forming the source bus line 25 is formed disconnected and each end 25b of a unit pattern 25a is formed to extend parallel to the gate bus line 21.

The gate electrode 33 is formed elongated parallel to the source bus line 25 on the way of which two widened portions 33a and 33b are formed corresponding to TFTs 31 and 32.

[Second step]

The connected pattern (cross-hatched area in Fig. 4) of the gate bus line 21, the bypass bus line 22 and the gate electrode 33 is oxidized by the anodic oxidization method to form a thin insulation layer 41 of Ta_2O_5 with a thickness of 500 to 5,000 Å as shown in Figs. 4 and 5.

[Third step]

In this step, a gate insulator 42 of SiN_x with a thickness of 500 to 5,000 Å, a semiconductor layer 43 of a-Si (ni) with a thickness of 50 to 4,000 Å, an etching stopper layer 44 with a thickness of 300 to 5,000 Å are formed stacked successively by PCVD method, as shown in Fig. 7.

Thereafter, the uppermost layer 44 is processed by the photolithography to form island portions 45a, 45b, 46a and 46b as etching stoppers, as shown in Fig. 6 and indicated by cross-hatched areas partially in Fig. 8.

The island portions 45a and 45b correspond to TFTs 31 and 32 to be formed and the other two island portions 46a and 46b are provided for covering the crossing zone of the gate bus line 21 with the source bus line 25 and the bypass bus line 26 thereof.

[Fourth step]

Next, a thin layer 47 of a-Si (n^+) with a thickness of 200 to 2,000 Å is formed by PCVD method, as shown in Fig. 10. Then, the layer 47 is processed together with the layer 43 of a-Si(i) by photolithography so as to form island patterns 48a, 48b, 49a and 49b which cover the island portions 45a, 45b, 46a and 46b, respectively, as shown by cross-hatched areas in Fig. 9.

Namely, each of these island portions is comprised of double layers 47 and 43 of a-Si (n^+) and

a-Si(i), as shown in Fig. 11.

[Fifth step]

As shown in Fig. 12, a pair of through holes 53 are perforated at each portion of the gate bus line 21 from which the bypass gate bus line 22 is formed. Also, a pair of through holes 54 are perforated at each end corner of the unit pattern 25a for forming the source bus line 25.

Each of these through holes 53 and 54 is formed by photoetching the insulation layer 42 of SiN_x .

Each pair of through holes gives a kind of redundant structure for the through hole.

[Sixth step]

Next, a layer 55 of titanium with a thickness of 500 to 5,000 Å is deposited by sputtering so as to cover the whole area as shown in Fig. 15.

Then, the layer 55 of Ti is removed except for the cross-hatched areas shown in Fig. 14.

In this process, two parallel lines 56a and 56b are formed so as to connect two opposite end portions 25b of the unit patterns 25a for the source bus line 25. In other words, the first line 56a connects two adjacent unit patterns 25a to form the source bus line 25 and the second line 56b forms the bypass bus line 26 at the crossing zone 24.

Also, source electrodes 31g and 32g and drain electrodes 31d and 32d of TFTs 31 and 32 are formed, respectively.

Further, the layers of Ti formed on the gate bus line 21 and the source bus line 25 are electrically connected, through the through holes 53 and 54, to the portions of Ta film formed in the first step, as shown in Fig. 16.

Thus, the portion of the gate bus line 21 defined between two pairs of through holes 53 is doubled and, also, the portion of the unit pattern 25a for the source bus line 25 defined between two pairs of through holes 54 is doubled.

The double bus line structure gives a kind of redundant structure to each of the gate and source bus lines 21 and 25.

[Seventh step]

Next, indium oxide (ITO) is deposited over the whole area of the substrate to form a thin film 57 with a thickness of 300 to 3,000 Å, as shown in Fig. 18.

Then, as shown by cross-hatched areas in Fig. 17, the ITO film 57 is photoetched to form individ-

ual picture element electrodes 30. Portions of the ITO film 57 remaining on respective bus lines 21 and 25 contribute to avoid possible breaks of them which may be caused during the patterning process in the sixth step.

Fig. 20 shows a structure of layers cross-sectioned along II-II line of Fig. 1.

As disclosed above, various redundant structures are provided for avoiding possible image defects caused by breaks of bus lines and inoperative transistors.

Thus, the present invention is able to provide an active matrix substrate being stable in operation thereof.

The preferred embodiments described herein are illustrative and not restrictive, the scope of the invention being indicated by the appended claims and all variations which come within the meanings of the claims are intended to be embraced herein.

There are described above novel features which the skilled man will appreciate give rise to advantages. These are each independent aspects of the invention to be covered by the present application, irrespective of whether or not they are included within the scope of the following claims.

Claims

1. An active matrix substrate for the liquid crystal display comprising:
a transparent insulated substrate;
a plurality of gate bus lines being formed parallel to each other on a surface of said substrate;
a plurality of source bus lines being formed so as to cross said plurality of gate bus lines in such a manner that each source bus line is insulated from gate bus lines at respective crossing areas with the latter bus lines;
a plurality of transparent picture element electrodes each of which is formed in each area defined by adjacent gate bus lines and source bus lines; and
a switching means for connecting a picture element electrode to a source bus line corresponding thereto when it is designated by the corresponding gate and source bus lines being characterized in that:
a switching circuit for switching on each of picture elements which is comprised of the corresponding gate bus line, source bus line and the switching means includes at least one redundant structure for avoiding the inoperativeness of said switching circuit.

2. An active matrix substrate as claimed in claim 1, in which said gate bus line has a bypass bus line as said redundant structure, which bypasses a portion of said gate bus line inbetween the adjacent source bus line.

3. An active matrix substrate as claimed in claim 2, in which said gate bus line is formed double, when seen in the direction of the thickness thereof, at least in a range along which said bypass line is formed.

4. An active matrix substrate as claimed in claim 1, in which said source bus line has a bypass bus line as said redundant structure, which bypasses a portion of said source bus line at each crossing area with said gate bus line.

5. An active matrix substrate as claimed in claim 4, in which said source bus line is formed double, when seen in the direction of the thickness thereof, except for the crossing zone thereof with said gate bus line.

6. An active matrix substrate as claimed in claim 1, in which said switching means is comprised of two thin film transistors connected parallel between the source bus line and the picture element electrode so as to form said redundant structure.

7. An active matrix substrate for a matrix display of the kind in which an array of display elements is controlled by a corresponding array of switching means, each arranged to control the display state of a respective said display element, said substrate including an array of display element electrodes, a plurality of parallel source lines and, a plurality of parallel gate lines extending in a direction across said source lines, said switching means being also part of the substrate and each arranged to supply an energizing voltage to the associated display element electrode when a given source line/gate line pair connected to that switching means is selected, wherein for at least some of said display element electrodes, a switching circuit which comprises the respective switching means and associated portions of the gate and source lines in the region of said display element electrode also includes a redundancy element which normally duplicates the function of a part of said switching circuit.

8. A matrix display device in which an array of display elements are controlled by a corresponding array of switching circuits formed on a substrate which also carries electrodes of the display elements, a said switching circuit including a redundancy structure for inhibiting inoperativeness of said switching circuit.

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Fig.1

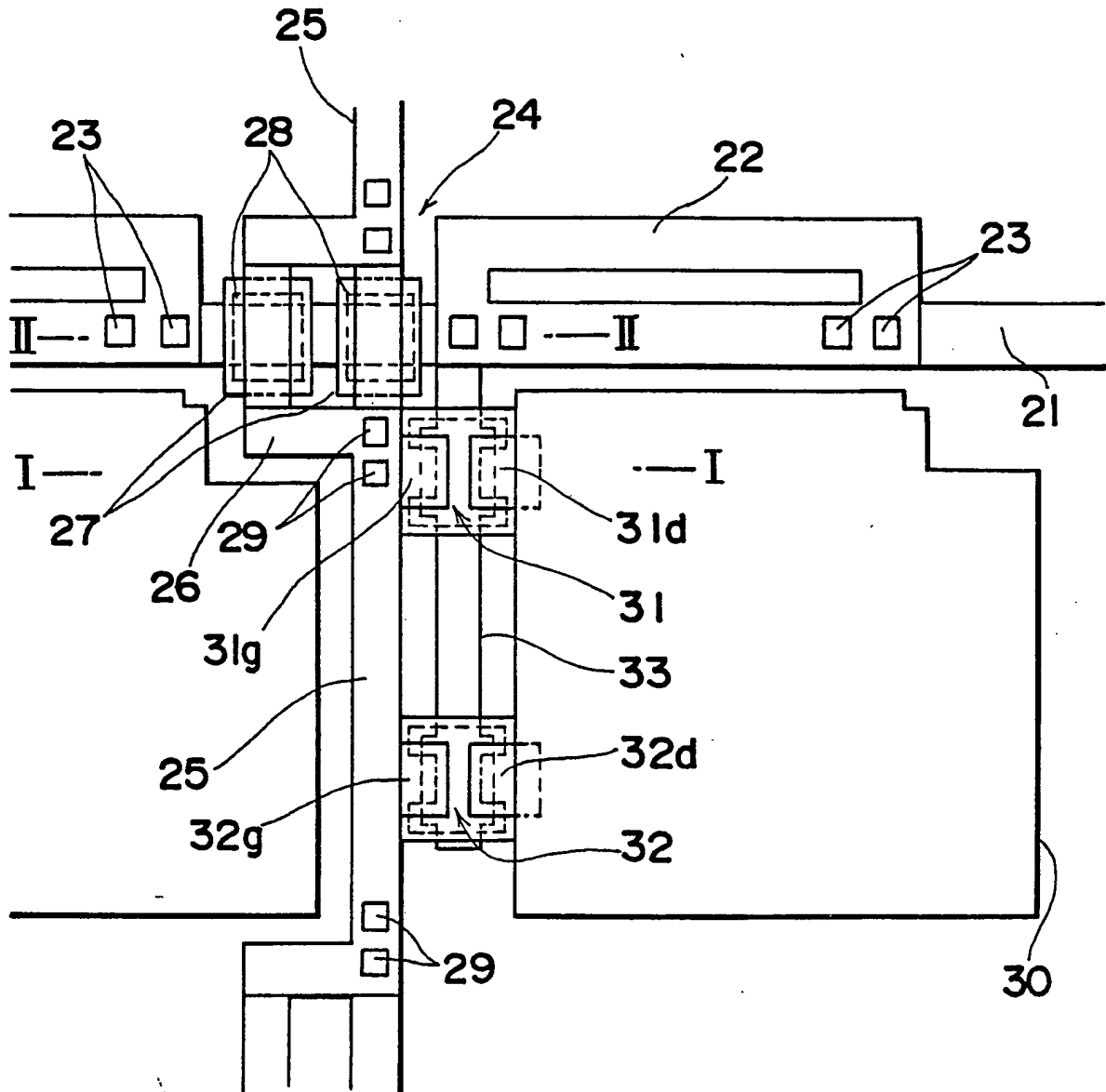


Fig.2

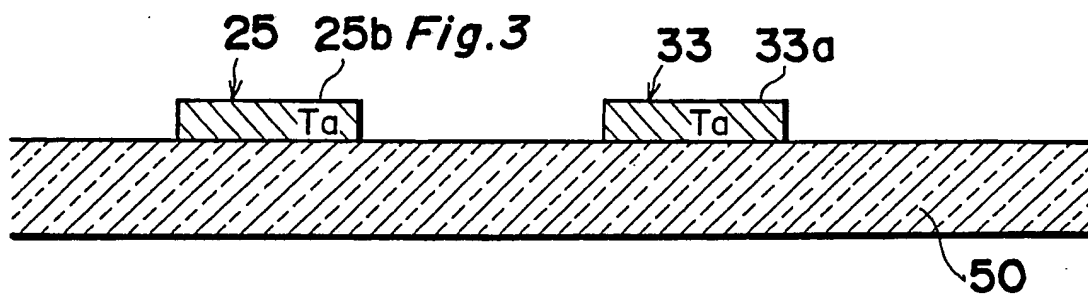
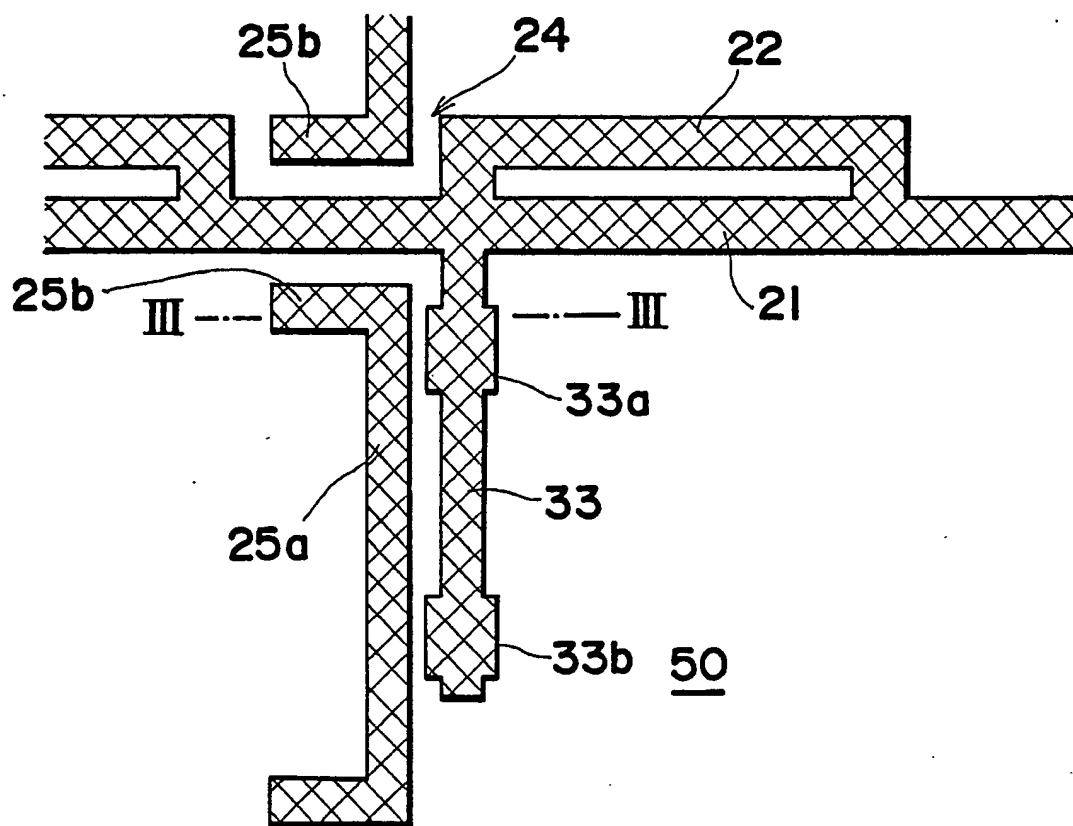


FIG. 4

Fig. 4

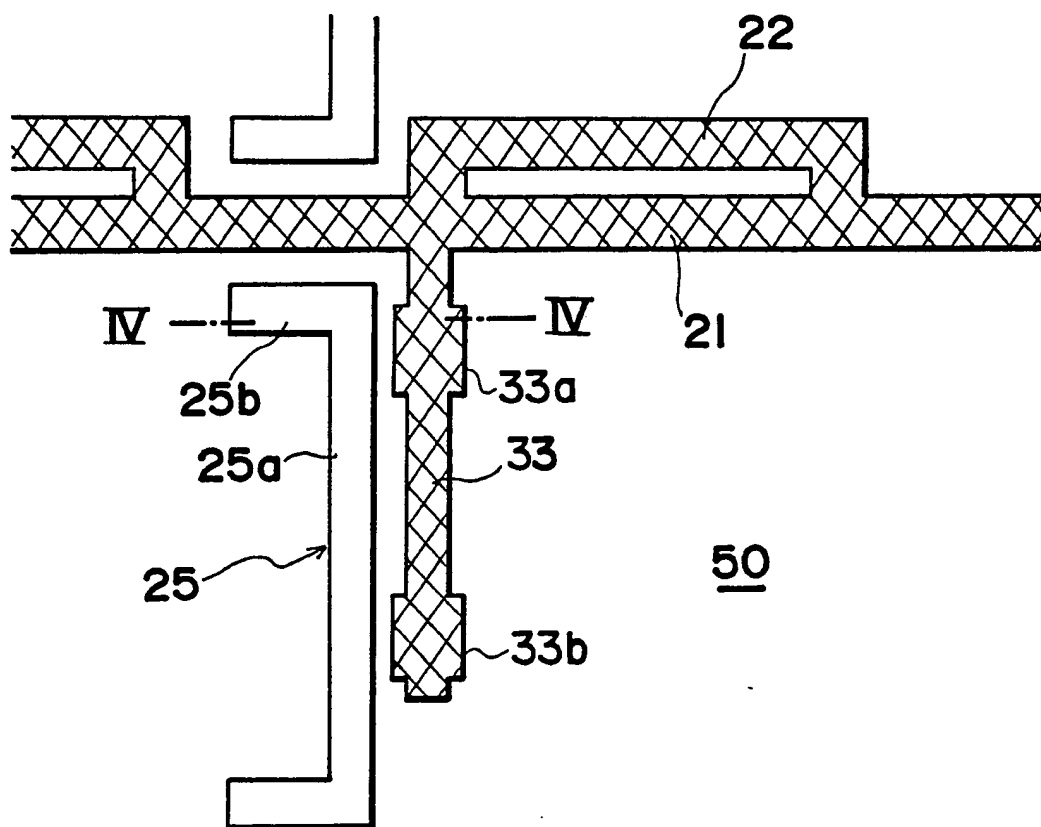


Fig. 5

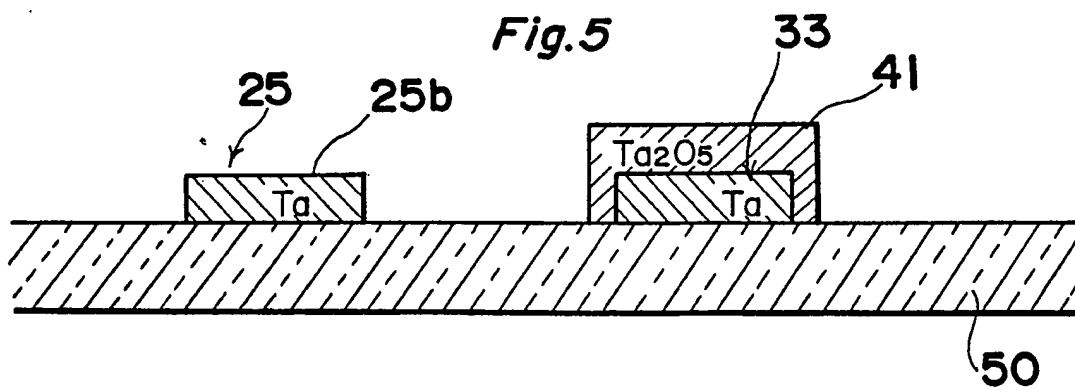


Fig.6

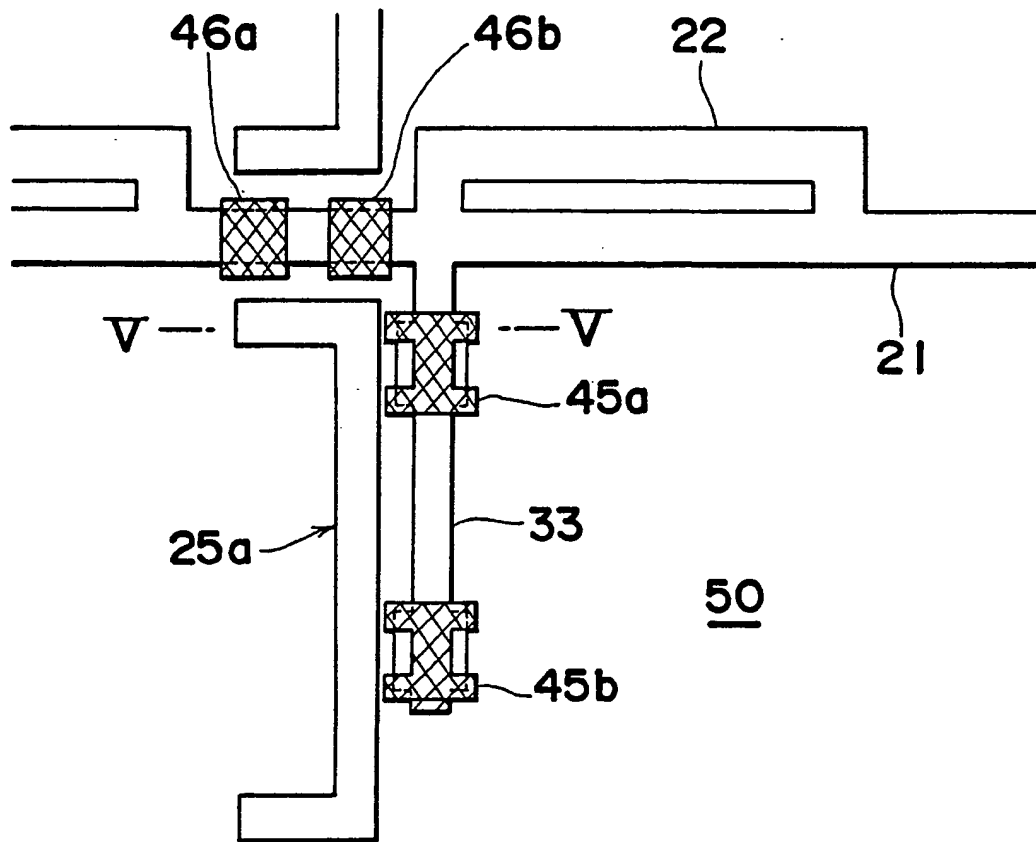


Fig.7

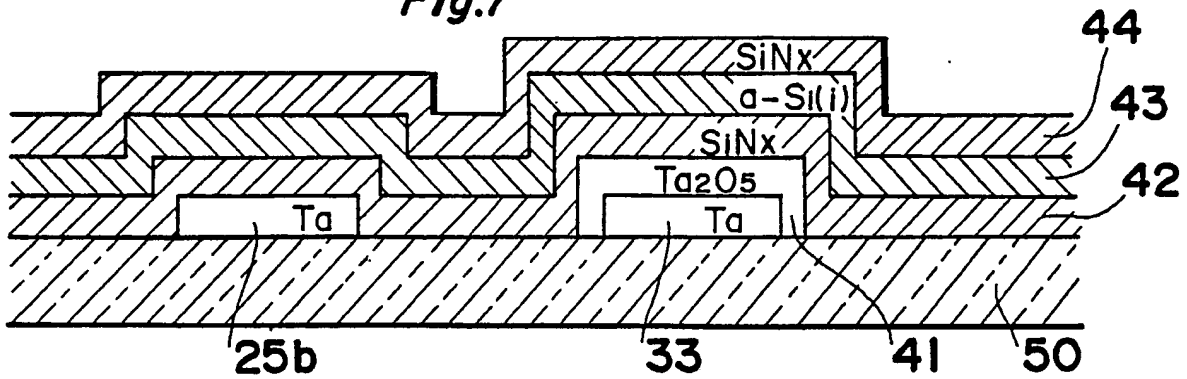


Fig.8

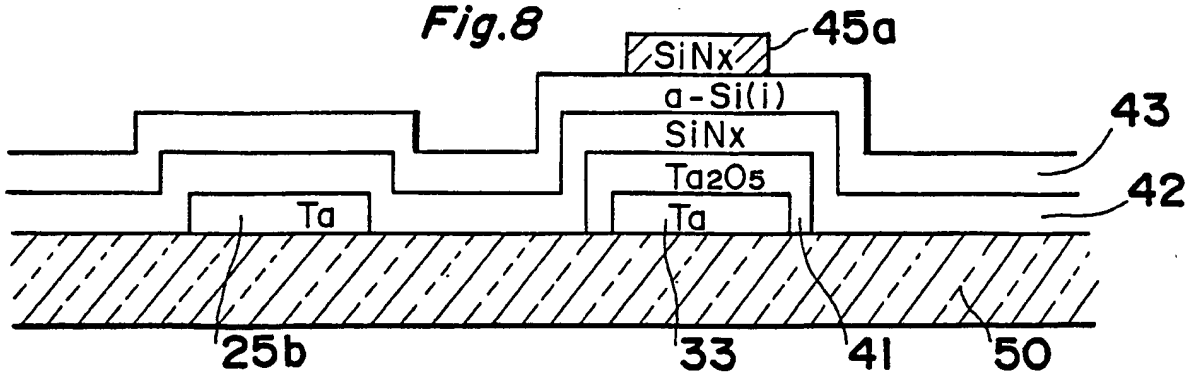


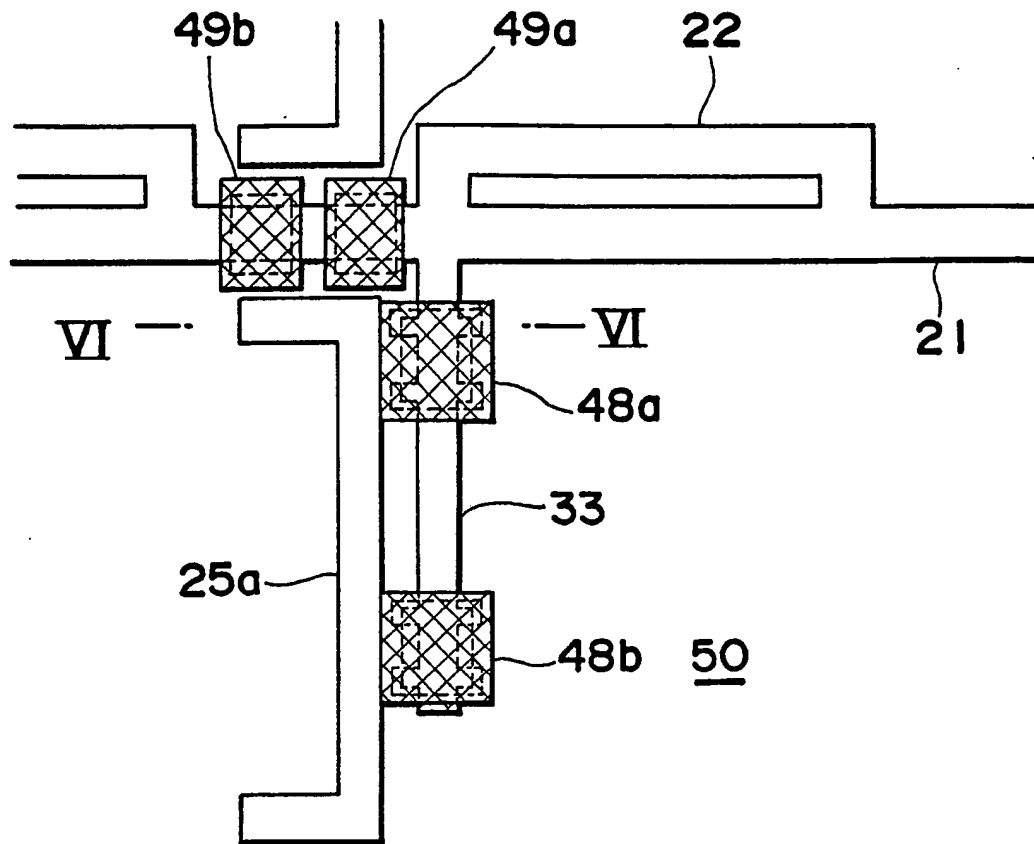
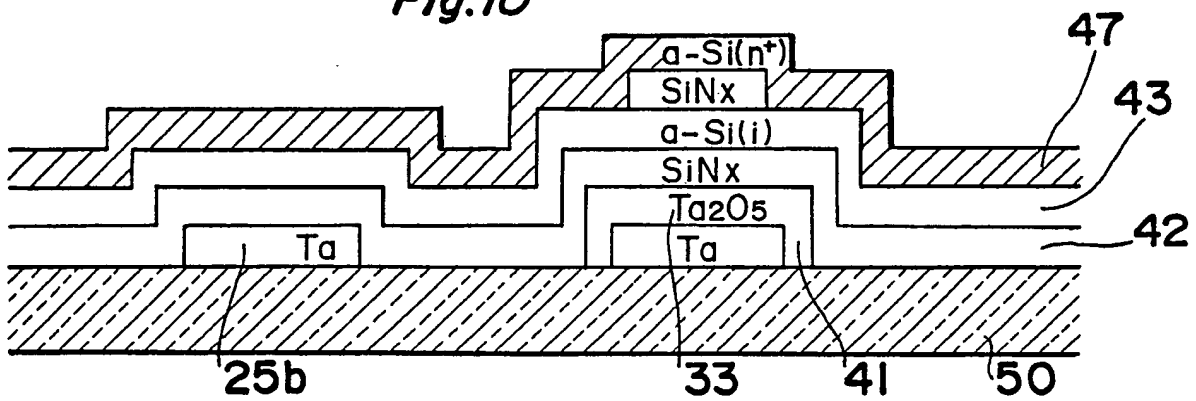
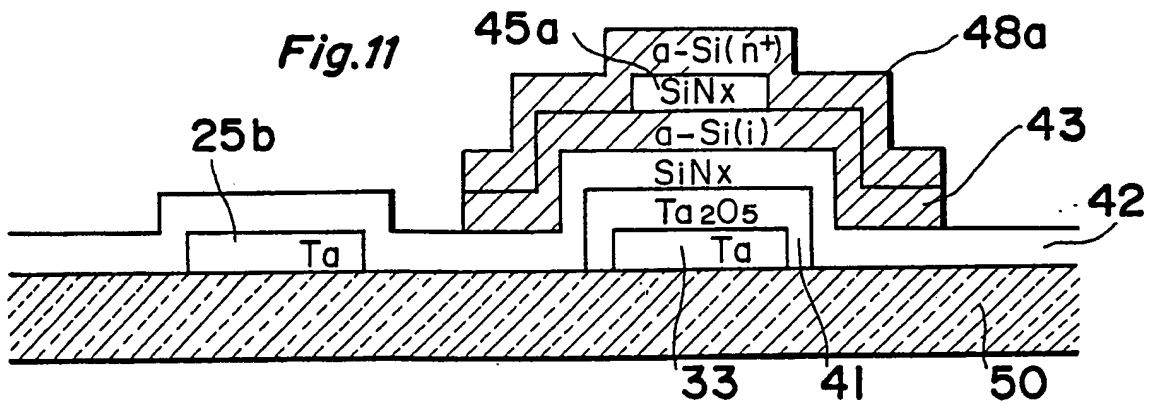
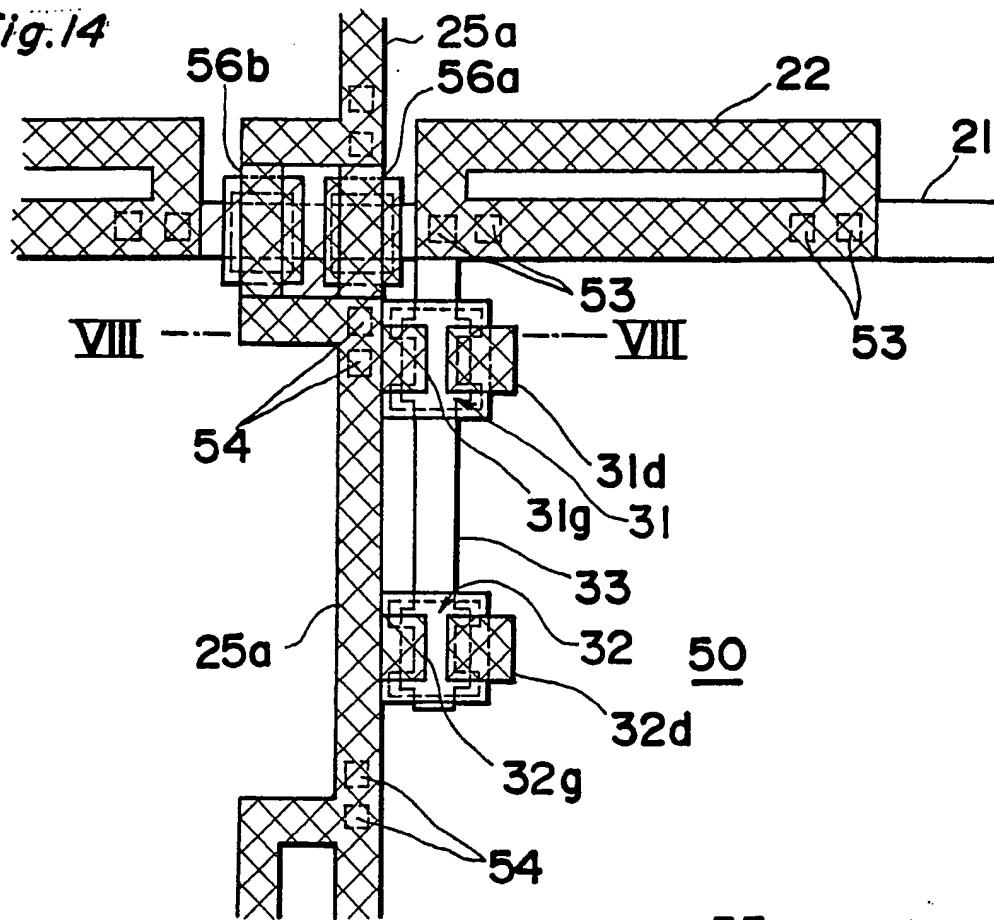
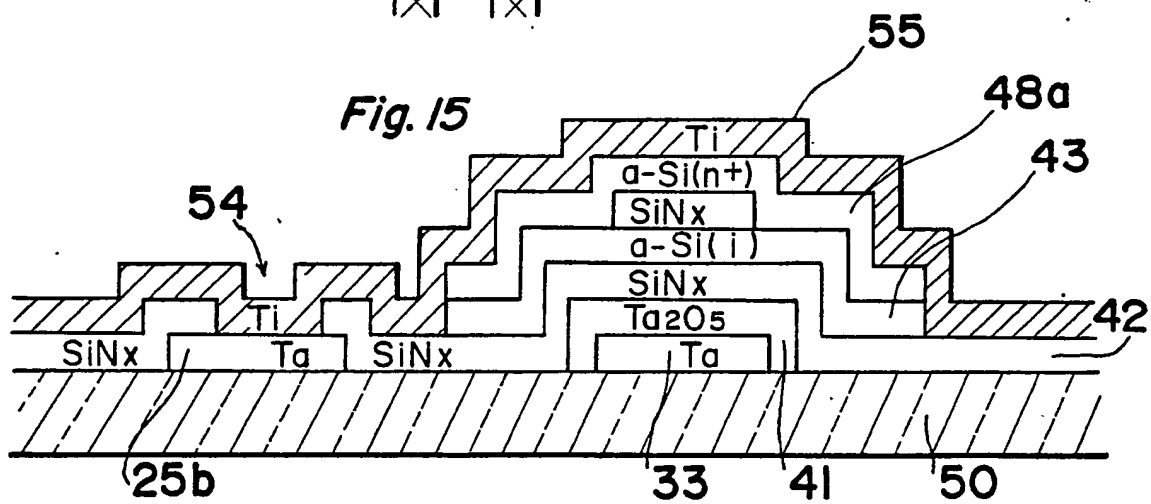
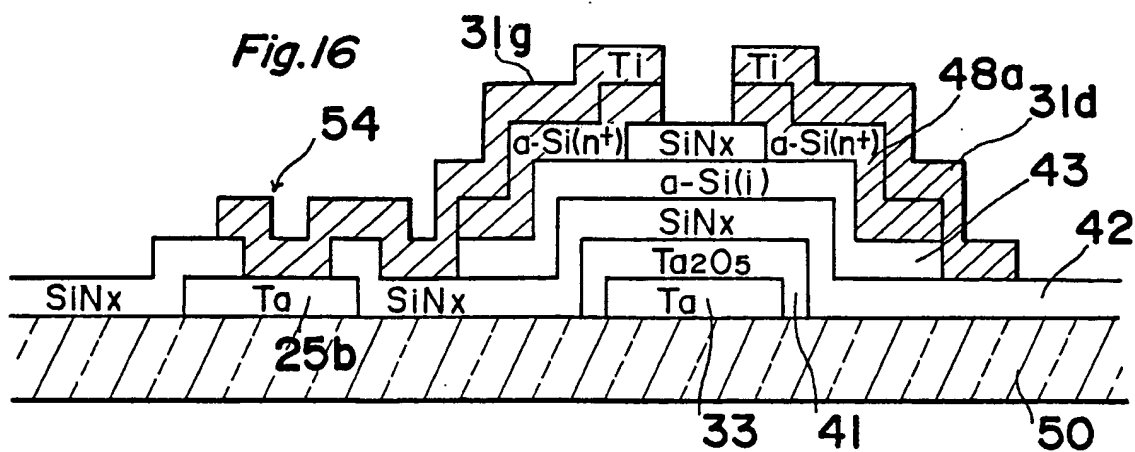
Fig.9**Fig.10****Fig.11**



Fig. 14**Fig. 15****Fig. 16**

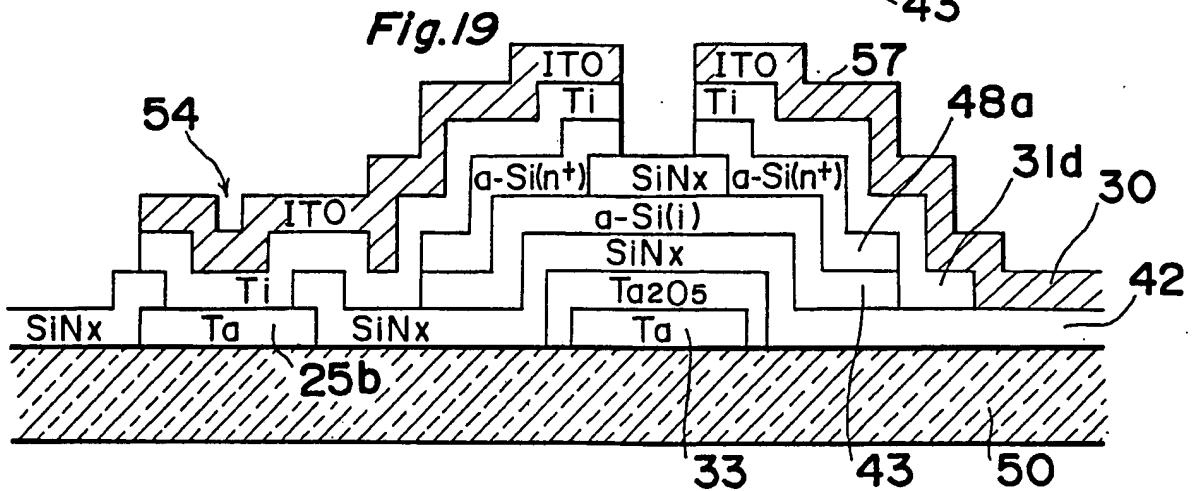
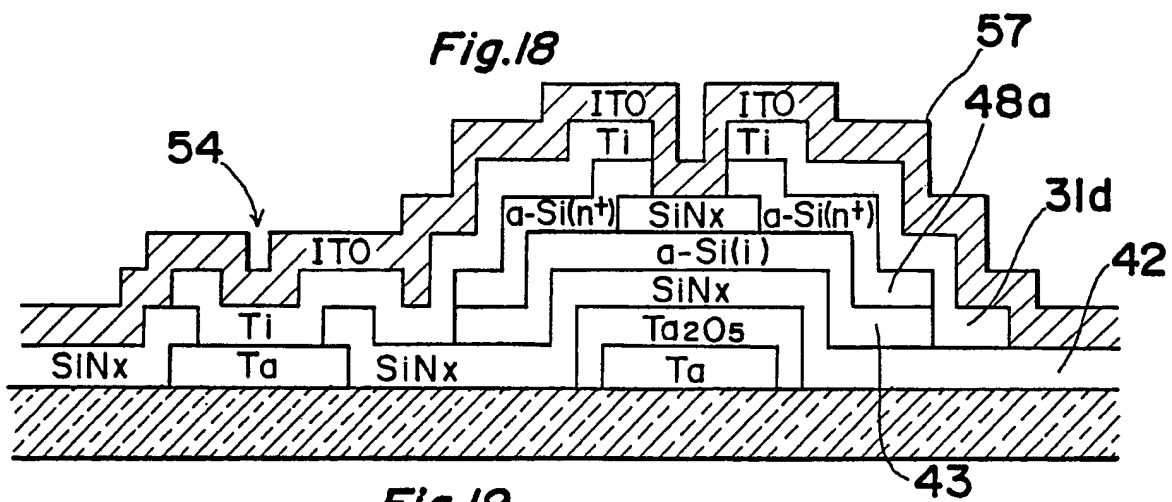
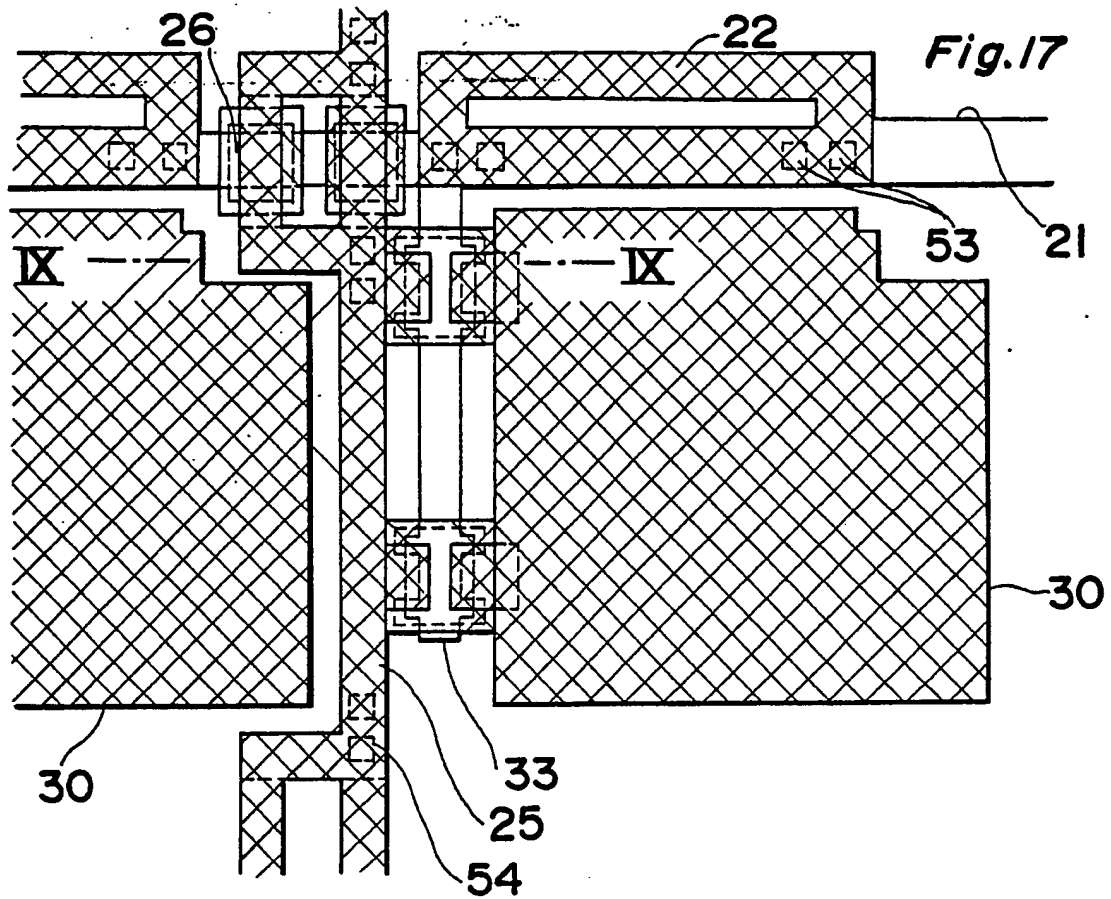


Fig. 21

	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈	Y _n
X ₁	A ₁₁	A ₁₂	A ₁₃	A ₁₄	A ₁₅	A ₁₆	A ₁₇	---	---
X ₂	A ₂₁	A ₂₂	A ₂₃	A ₂₄	A ₂₅	A ₂₆	A ₂₇	---	A _{2n}
X ₃	A ₃₁	A ₃₂	A ₃₃	A ₃₄	A ₃₅	A ₃₆	A ₃₇	---	A _{3n}
X ₄	A ₄₁	A ₄₂	A ₄₃	A ₄₄	A ₄₅	A ₄₆	A ₄₇	---	A _{4n}
X ₅	A ₅₁	A ₅₂	A ₅₃	A ₅₄	A ₅₅	A ₅₆	A ₅₇	---	A _{5n}
X ₆	A ₆₁	A ₆₂	A ₆₃	A ₆₄	A ₆₅	A ₆₆	A ₆₇	---	A _{6n}
X ₇	A ₇₁	A ₇₂	A ₇₃	A ₇₄	A ₇₅	A ₇₆	A ₇₇	---	A _{7n}
X ₈	---	---	---	---	---	---	---	---	---
...	---	---	---	---	---	---	---	---	---
X _m	A _{m1}	A _{m2}	A _{m3}	A _{m4}	A _{m5}	A _{m6}	A _{m7}	---	A _{mn}

Fig. 22

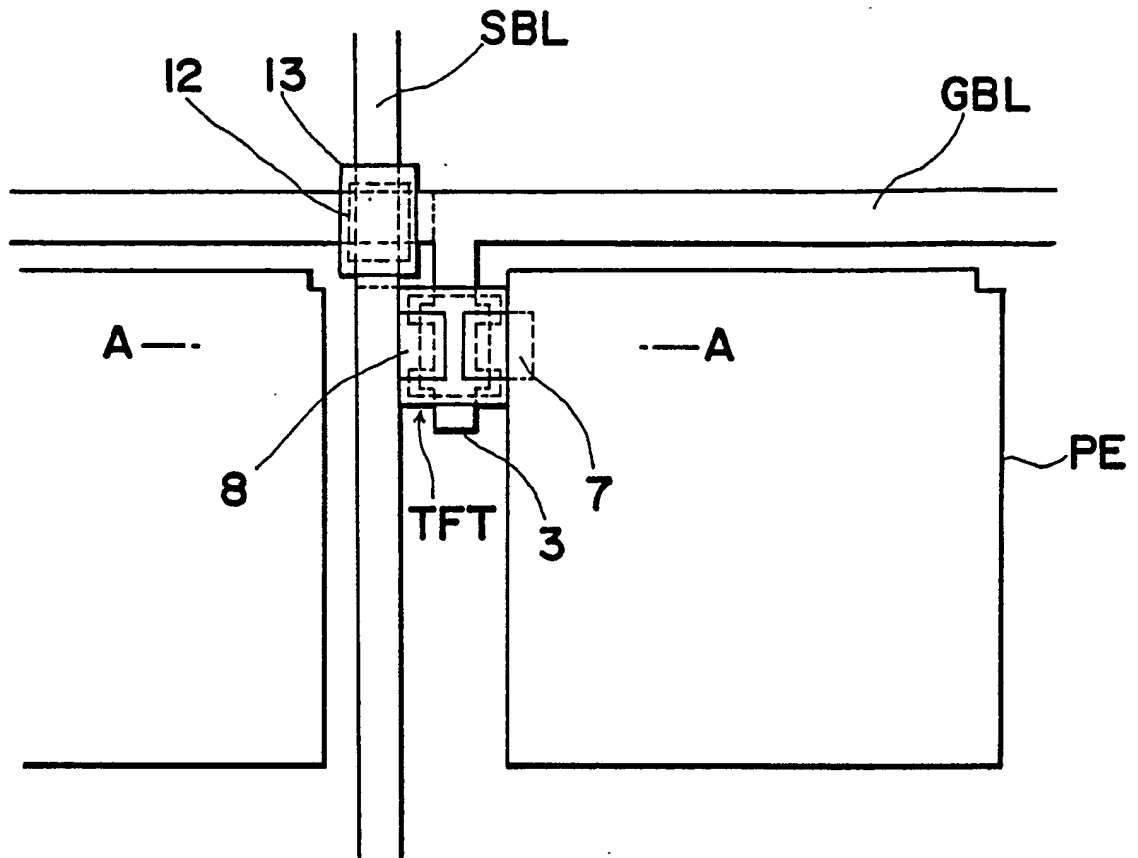
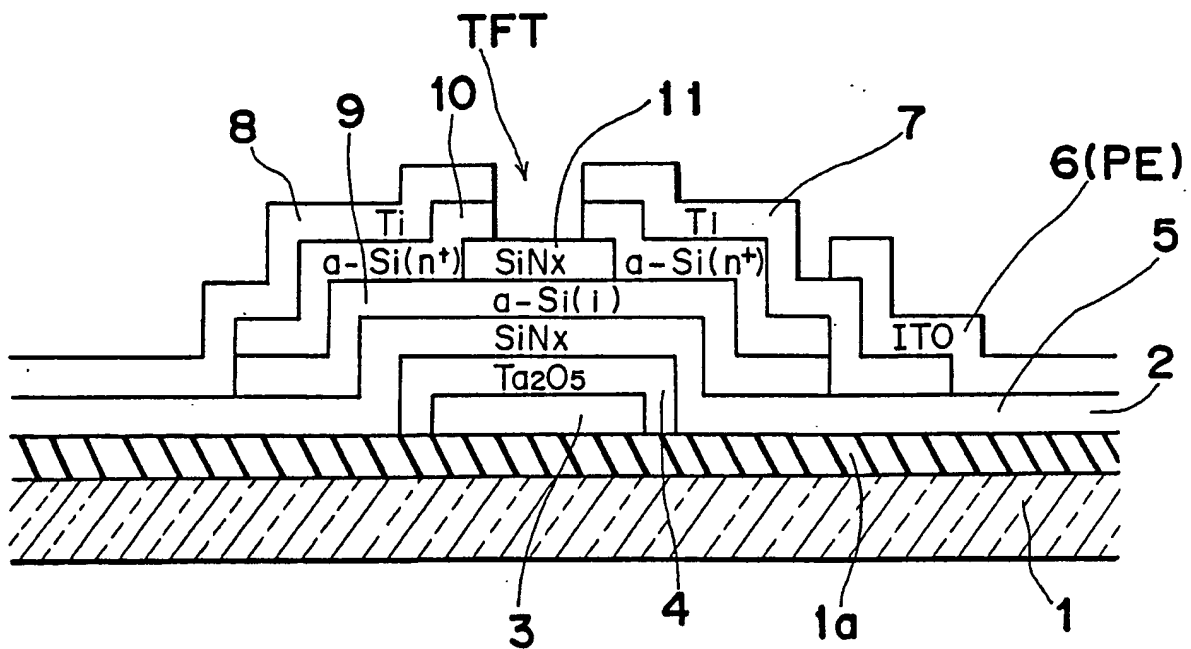


Fig. 23



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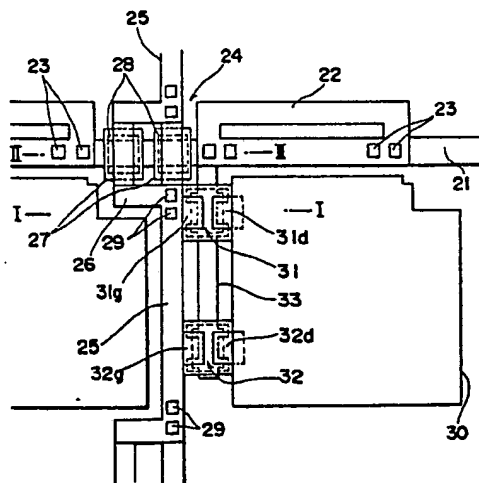
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Fig.1



EP 0 318 224 A3



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	JP-A-61 249 078 * Whole document * ---	1-8	G 02 F 1/133
X	EP-A-0 209 113 (GENERAL ELECTRIC) * Abstract; figures * ---	1,7,8	
X	EP-A-0 200 138 (ASAHI GLASS) * Column 8, lines 17-38; figures 4,5 * ---	1,7,8	
A	PATENT ABSTRACTS OF JAPAN, vol. 9, no. 214 (P-384)[1937], 31th August 1985; & JP-A-60 073 617 (TOSHIBA K.K.) 25-04-1985 * Whole document * ---	1,7,8	
A	FR-A-2 582 431 (MITSUBISHI) * Figures * -----	1,7,8	
			TECHNICAL FIELDS SEARCHED (Int. Cl.4)
			G 02 F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 22-01-1990	Examiner LOFFREDO A.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			



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214 (P-384)[1937], 31th August 1985; & JP-
A-60 073 617

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EP 0 318 224 B1

Description

The present invention relates to an active matrix substrate, such as may be used for a liquid crystal display on which a switching matrix using thin film transistors is formed to drive individual picture elements.

The liquid crystal display having picture elements arranged in a matrix form, as shown in Fig. 21 schematically, is widely used. Especially, the liquid crystal display panel is widely used for the display of an electronic apparatus such as a personal computer of lap-top type or the like.

In a recent liquid crystal display panel, a so-called active matrix substrate is used on which a number of thin film transistors are formed in a matrix form. As shown in Fig. 22 schematically, each thin film transistor (TFT) switches on the corresponding transparent electrode PE for a picture element when designated through both the gate and the source bus lines GBL and SBL.

Fig. 23 shows a cross-sectional view along line A-A of Fig. 22.

An insulation film 1a is formed on a glass substrate 1, and a gate electrode 3 is formed together with the gate bus line GBL on the insulation film 1a by etching Ta film.

This gate electrode 3 and the gate bus line GBL are covered with an anodic oxide film 4 of Ta₂O₅ and a gate insulator 5 of SiNx is formed so as to cover whole of the former insulation film 1a including the anodic oxide film 4. On the area of the gate insulator 5 covering the anodic oxide film 4, a thin film transistor TFT is formed to switch on a transparent electrode 6 for each of the picture elements formed on the gate insulator 5. The thin film transistor TFT is formed so as to have a drain electrode 7 connected to the picture element electrode 6, a source electrode 8 connected to the source bus line SBL, and a semiconductor film 9 of amorphous silicon (a-Si) formed above the gate electrode 3. This semiconductor film 9 is connected to the drain electrode 7 and the source electrode 8 through a film 10 of amorphous silicon and is covered by a protection film 11.

According to this structure, the TFT is switched on by applying a predetermined voltage to the gate electrode 3 through the gate bus line GBL and, therefore, a voltage applied to the source bus line SBL is applied to the picture element electrode 6 through the a-Si semiconductor film 9.

The gate bus line GBL and the source bus line SBL are insulated from each other at their crossing zone by an a-Si (i)/a-Si (n⁺) layer 12 and covered by an etching stopping layer 13.

In such a structure of the active matrix substrate, if a gate bus line GBL or a source bus line SBL is broken, all of the picture element electrodes

aligned along the broken bus line become inactive to cause a line defect of an image to be displayed. Also, if a TFT is broken, the corresponding picture element is made inactive.

Conventionally, various efforts regarding the production process have been made in order to avoid these defects. However, it is impossible to avoid them completely only by improving the production process.

From EP-A-0,209,113, there is known a liquid crystal display device in which redundancy is provided in the source and gate lines which drive the picture element transistors. Each line comprises two conductive layers which, in the case of the source line, sandwich a narrow insulating strip. The two conductive layers make contact along the edges of the insulating strip.

EP-A-0,200,138 and JP-A-61-249,078, on the other hand, disclose display substrates in which redundancy is provided by two or more transistors for switching each picture element.

One of the objects of the present invention is to provide a structure of the active matrix substrate for liquid crystal display which is capable of minimising possible image defects such as line defects, picture element defects and the like.

Another object of the present invention is to provide a structure of the active matrix substrate which is capable of preventing possible line defects caused by bus line breaks.

A further object of the present invention is to provide a structure of the active matrix substrate which is capable of preventing possible picture element defects due to inoperative TFTs.

The invention provides an active matrix display substrate including an array of picture element electrodes, a respective switching means associated with each picture element electrode, a plurality of parallel source lines, and a plurality of parallel gate lines extending in a direction across said source lines and insulated therefrom, each switching means enabling its associated picture element electrode to be energized by the application of signals to a given source line/gate line pair connected to the switching means, wherein each of said source lines and each of said gate lines has a double-layered structure at line portions which extend along the length of the line in-between the source line/gate line cross-over regions, said double-layered structure comprising two conductive layers which overlie each other and are electrically connected, characterised in that each gate line includes gate bypass line portions which bypass the gate line in-between said cross-over regions, and each source line includes source bypass line portions which bypass the source line at said cross-over regions.

The present invention will become more apparent when a preferred embodiment thereof is described in detail with reference to the accompanying drawings, in which:

Fig. 1 is an explanatory enlarged plan view of a portion of the active matrix substrate according to the present invention;

Fig. 2 is an explanatory enlarged plan view for showing the first step of the production process of the active matrix substrate;

Fig. 3 is a schematic cross-sectional view along line III-III of Fig. 2;

Fig. 4 is an explanatory enlarged plan view for showing the second step of the production process;

Fig. 5 is a schematic cross-sectional view along line IV-IV of Fig. 4;

Fig. 6 is an explanatory enlarged plan view for showing the third step of the production process;

Fig. 7 is a schematic cross-sectional view along line V-V of Fig. 6;

Fig. 8 is a schematic cross-sectional view along line V-V of Fig. 6 for showing the result obtained by performing the third step;

Fig. 9 is an explanatory enlarged plan view for showing the fourth step of the production process;

Fig. 10 is a schematic cross-sectional view along line VI-VI of Fig. 9;

Fig. 11 is a schematic cross-sectional view along line VI-VI of Fig. 9 for showing the result obtained by performing the fourth step;

Fig. 12 is an explanatory enlarged plan view for showing the fifth step of the production process;

Fig. 13 is a schematic cross-sectional view along line VII-VII of the Fig. 12;

Fig. 14 is an explanatory enlarged plan view for showing the sixth step of the production process;

Fig. 15 is a schematic cross-sectional view along line VIII-VIII of Fig. 14;

Fig. 16 is a schematic cross-sectional view along line VIII-VIII of Fig. 14 for showing the result obtained by performing the sixth step;

Fig. 17 is an explanatory enlarged plan view for showing the seventh step of the production process;

Fig. 18 is a schematic cross-sectional view along line IX-IX of Fig. 17;

Fig. 19 is a schematic cross-sectional view along line IX-IX of Fig. 17 for showing the result obtained by performing the seventh step of the production process;

Fig. 20 is a schematic cross-sectional view along line II-II of Fig. 1;

Fig. 21 is a schematic plan view showing an active matrix substrate;

Fig. 22 is a schematic enlarged plan view showing a portion of a conventional active matrix substrate; and

Fig. 23 is a schematic cross-sectional view along line A-A of Fig. 22.

Fig. 1 shows an enlarged plan view of a portion of the active matrix substrate according to a preferred embodiment of the present invention.

As shown in Fig. 1, a gate bus line 21 and a source bus line 25 are formed so as to cross at right angles. A transparent picture element electrode 30 is formed in each square area defined by two adjacent bus lines and two adjacent source bus lines. Each picture element electrode 30 is switched on or off to the source bus line 25 by two thin film transistors (TFTs) 31 and 32.

These two TFTs 31 and 32 are arranged parallel on a gate electrode 33 which is formed so as to extend parallel to the source bus line 25 on an area defined between the same and the picture element electrode 30.

In the present preferred embodiment, various redundant structures are provided for the gate bus line 21, the source bus line 25 and the switching structure of each picture element electrode 30.

With respect to the gate bus line 21, there is provided a bypass bus line 22 at every picture element electrode 30 which extends parallel to the gate bus line 21 and is terminated before the crossing zone 24 with the source bus line 25.

Further, the part of the gate bus line 21 parallel to the bypass bus line 22 and the latter are made as a double layered structure, as will be explained later.

With respect to the source bus line 25, a bypass bus line 26 which bypasses the crossing portion thereof with the gate bus line 21 is formed at the crossing zone 24 and the remaining portion thereof except for the crossing zone is made as a double layered structure.

With respect to the switching structure for each picture element electrode 30, each gate electrode 33 is formed elongated parallel to both the source bus line 25 and the side of the picture element electrode 30 and two TFTs 31 and 32 are formed parallelly on the gate electrode 33, which are able to switch on and off the picture element electrode 30 to the source bus line 25, as mentioned above.

Hereinafter, these redundant structures will be explained more concretely together with the production process of the active matrix substrate.

First Step

At first, as shown in Fig. 3, a thin film of tantalum (Ta) with a thickness of 500 to 5,000 Å is deposited on a surface of an insulated glass substrate 50.

Then, as indicated as cross-hatched areas in Figs. 2 and 3, individual patterns corresponding to the gate bus line 21, the bypass bus line 22 thereof, the source bus line 25 and the gate electrode 33 are formed by photoetching the tantalum film. The bypass bus line 22 is formed parallel to the gate bus line 21 and terminated before the crossing zone 24 in order not to increase possible leak and stray capacitance between two bus lines 21 and 25.

In this step, the pattern for forming the source bus line 25 is formed disconnected and each end 25b of a unit pattern 25a is formed to extend parallel to the gate bus line 21.

The gate electrode 33 is formed elongated parallel to the source bus line 25 on the way of which two widened portions 33a and 33b are formed corresponding to TFTs 31 and 32.

Second Step

The connected pattern (cross-hatched area in Fig. 4) of the gate bus line 21, the bypass bus line 22 and the gate electrode 33 is oxidized by the anodic oxidization method to form a thin insulation layer 41 of Ta_2O_5 with a thickness of 500 to 5,000 Å, as shown in Figs. 4 and 5.

Third Step

In this step, a gate insulator 42 of SiN_x with a thickness of 500 to 5,000 Å, a semiconductor layer 43 of a-Si (i) with a thickness of 50 to 4,000 Å, and an etching stopper layer 44 with a thickness of 300 to 5,000 Å are formed stacked successively by PCVD method, as shown in Fig. 7.

Thereafter, the uppermost layer 44 is processed by photolithography to form island portions 45a, 45b, 46a and 46b as etching stoppers, as shown in Fig. 6 and indicated by cross-hatched areas partially in Fig. 8.

The island portions 45a and 45b correspond to TFTs 31 and 32 to be formed and the other two island portions 46a and 46b are provided for covering the crossing zone of the gate bus line 21 with the source bus line 25 and the bypass bus line 26 thereof.

Fourth Step

Next, a thin layer 47 of a-Si (n^+) with a thickness of 200 to 2,000 Å is formed by PCVD method, as shown in Fig. 10. Then, the layer 47 is processed together with the layer 43 of a-Si(i) by photolithography so as to form island patterns 48a, 48b, 49a and 49b which cover the island portions 45a, 45b, 46a and 46b, respectively, as shown by cross-hatched areas in Fig. 9.

Namely, each of these island portions is composed of double layers 47 and 43 of a-Si (n^+) and a-Si(i), as shown in Fig. 11.

Fifth Step

As shown in Fig. 12, a pair of through holes 53 are perforated at each portion of the gate bus line 21 from which the bypass gate bus line 22 is formed. Also, a pair of through holes 54 are perforated at each end corner of the unit pattern 25a for forming the source bus line 25.

Each of these through holes 53 and 54 is formed by photoetching the insulation layer 42 of SiN_x .

Each pair of through holes gives a kind of redundant structure for the through hole.

Sixth Step

Next, a layer 55 of titanium with a thickness of 500 to 5,000 Å is deposited by sputtering so as to cover the whole area as shown in Fig. 15.

Then, the layer 55 of Ti is removed except for the cross-hatched areas shown in Fig. 14.

In this process, two parallel lines 56a and 56b are formed so as to connect the two opposite end portions 25b of the unit pattern 25a for the source bus line 25. In other words, the first line 56a connects two adjacent unit patterns 25a to form the source bus line 25 and the second line 56b forms the bypass bus line 26 at the crossing zone 24.

Also, source electrodes 31g and 32g and drain electrodes 31d and 32d of TFTs 31 and 32 are formed, respectively.

Further, the layers of Ti formed on the gate bus line 21 and the source bus line 25 are electrically connected, through the through holes 53 and 54, to the portions of Ta film formed in the first step, as shown in Fig. 16 (for the source bus line).

Thus, the portion of the gate bus line 21 defined between two pairs of through holes 53 is doubled and, also, the portion of the unit pattern 25a for the source bus line 25 defined between two pairs of through holes 54 is doubled.

The double bus line structure gives a kind of redundant structure to each of the gate and source bus lines 21 and 25.

Seventh Step

Next, indium tin oxide (ITO) is deposited over the whole area of the substrate to form a thin film 57 with a thickness of 300 to 3,000 Å, as shown in Fig. 18.

Then, as shown by cross-hatched areas in Fig. 17, the ITO film 57 is photoetched to form individual picture element electrodes 30. Portions of the

ITO film 57 remaining on respective bus lines 21 and 25 contribute to avoid possible breaks of them which may be caused during the patterning process in the sixth step.

Fig. 20 shows a structure of layers cross-sectioned along line II-II of Fig. 1.

As discussed above, various redundant structures are provided for avoiding possible image defects caused by breaks of bus lines and inoperative transistors.

Thus, the present invention is able to provide an active matrix substrate being stable in operation thereof.

The preferred embodiments described herein are illustrative and not restrictive, the scope of the invention being indicated by the appended claims and all variations which come within the meanings of the claims are intended to be embraced herein.

Claims

1. An active matrix display substrate including an array of picture element electrodes (30), a respective switching means (31, 32) associated with each picture element electrode, a plurality of parallel source lines (25), and a plurality of parallel gate lines (21) extending in a direction across said source lines and insulated therefrom, each switching means enabling its associated picture element electrode to be energized by the application of signals to a given source line/gate line pair connected to the switching means, wherein each of said source lines (25) and each of said gate lines (21) has a double-layered structure at line portions which extend along the length of the line in-between the source line/gate line cross-over regions (24), said double-layered structure comprising two conductive layers (25, 55; 21, 55) which overlie each other and are electrically connected, characterised in that each gate line (21) includes gate bypass line portions (22) which bypass the gate line in-between said cross-over regions (24), and each source line (25) includes source bypass line portions (26) which bypass the source line at said cross-over regions (24).
2. An active matrix display substrate according to claim 1, wherein the two conductive layers (25, 55; 21, 55) of each line portion are connected together by through-hole connection (54; 53) through an insulating layer (42; 41, 42) formed therebetween.
3. An active matrix display substrate according to claim 2, wherein said through-hole connection comprises a pair of through-holes (53; 54)

formed in said insulating layer (41, 42; 42) at each end of the line portion (21; 25).

4. An active matrix display substrate according to any one of claims 1 to 3, wherein said gate bypass line portions (22) have said double-layered structure.
5. An active matrix display substrate according to any one of the preceding claims, wherein portions of an ITO film layer (57) deposited to form said picture element electrodes (30) cover one of the conductive layers (55) of the gate and source line portions.
6. An active matrix display substrate according to any one of the preceding claims, wherein said switching means comprises two thin-film transistors (31, 32) connected in parallel to the associated source line/gate line pair.

Patentansprüche

1. Aktives Matrix-Anzeigeeinrichtungs-Substrat, umfassend eine Anordnung von Bildelement-Elektroden (30), eine entsprechende Schaltvorrichtung (31, 32), die jeder Bildelement-Elektrode beigeordnet ist, eine Vielzahl von parallelen Quellenleitungen (25) und eine Vielzahl von parallelen Gateleitungen (21), die sich in einer Richtung quer über die genannten Quellenleitungen erstrecken und davon isoliert sind, wobei jede Schaltvorrichtung seine beigeordnete Bildelementelektrode durch die Anwendung von Signalen auf ein gegebenes Quellenleitungs/Gateleitungs-Paar, das mit der Schaltvorrichtung verbunden ist, zur Aktivierung befähigt, worin jede der Quellenleitungen (25) und jede der Gateleitungen (25), eine Doppelschicht-Struktur an den Leitungsteilen aufweist, die sich entlang der Länge der Leitung zwischen den Quellenleitungs/Gateleitungs-Überkreuzungsbereichen (24) erstreckt, wobei die Doppelschicht-Struktur zwei leitende Schichten (25, 55; 21, 55) umfaßt, die sich einander überlagern und elektrisch verbunden sind, dadurch gekennzeichnet, daß jede Gateleitung (21) Nebenschlußleitungs-Bereiche (22) umfaßt, die die Gateleitung zwischen den Überkreuzungsbereichen (24) überbrücken und jede Quellenleitung (25) Quellen-Nebenschlußleitungs-Bereiche (26) umfaßt, die die Quellenleitung an den Überkreuzungsbereichen (24) überbrücken.
2. Aktives Matrix-Anzeigeeinrichtungs-Substrat nach Anspruch 1, worin die zwei leitenden Schichten (25, 55; 21, 55) jedes Leitungsbe-

reichs durch Durchkontaktloch-Verbindungen (54; 53) durch eine Isolierschicht (42; 41, 42), die dazwischen ausgebildet ist, zusammen verbunden sind.

3. Aktives Matrix-Anzeigeeinrichtungs-Substrat nach Anspruch 2, worin die Durchkontaktloch-Verbindung ein Durchkontaktloch-Paar (53; 54) umfaßt, das in der Isolierschicht (41, 42; 42) an jedem Ende der Leitungsbereiche (21; 25) ausgebildet ist.

4. Aktives Matrix-Anzeigeeinrichtungs-Substrat nach einem der Ansprüche 1 bis 3, worin die Nebenschluß-Gateleitungs-Bereiche (22) diese Doppelschicht-Struktur aufweisen.

5. Aktives Matrix-Anzeigeeinrichtungs-Substrat nach einem der vorhergehenden Ansprüche, worin Bereiche einer ITO-Filmschicht (57), die zur Bildung der Bildelement-Elektroden abgeschieden wurden, eine der leitenden Schichten (55) der Gate- und Quellenleitungsbereiche bedecken.

6. Aktives Matrix-Anzeigeeinrichtungs-Substrat nach einem der vorhergehenden Ansprüche, worin die Schaltungsvorrichtung zwei Dünnschicht-Transistoren (31, 32) umfaßt, die parallel zu dem beigeordneten Quellenleitungs/Gateleitungs-Paar geschaltet sind.

Revendications

1. Substrat à matrice active pour un dispositif d'affichage, comprenant un réseau d'électrodes d'élément d'image (30), des moyens de commutation respectifs (31, 32) associés à chacune des électrodes d'élément d'image, une multiplicité de lignes de source parallèles (25), et une multiplicité de lignes de grille parallèles (21) qui s'étendent dans une direction transversale auxdites lignes de source et sont isolées par rapport à celles-ci, chacun des moyens de commutation autorisant l'excitation de son électrode d'élément d'image associée, par l'application de signaux à une paire donnée ligne de source/ligne de grille, connectée au moyen de commutation, dans lequel chacune desdites lignes de source (25) et chacune desdites lignes de grille (21) présente une structure à deux couches sur des tronçons de ligne qui s'étendent dans le sens de la longueur de la ligne, entre les régions (24) de croisement d'une ligne de source et d'une ligne de grille, ladite structure à deux couches comprenant deux couches conductrices (25, 55; 21, 55) qui se recouvrent l'une l'autre et

sont électriquement connectées entre elles, caractérisé en ce que chacune des lignes de grille (21) comprend des tronçons de ligne de contournement de grille (22) qui contournent la ligne de grille entre lesdites régions de croisement (24), et chacune des lignes de source (25) comprend des tronçons de ligne de contournement de source (26) qui contournent la ligne de source au niveau desdites régions de croisement (24).

2. Substrat à matrice active pour un dispositif d'affichage, selon la revendication 1, dans lequel les deux couches conductrices (25, 55; 21; 55) de chacun des tronçons de ligne sont raccordées l'une à l'autre par des connexions à trous traversants (54; 53) réalisées à travers une couche isolante (42; 41, 42) formée entre elles.

3. Substrat à matrice active pour un dispositif d'affichage, selon la revendication 2, dans lequel ladite connexion à trous traversants comprend une paire de trous traversants (53; 54), formée dans ladite couche isolante (41, 42; 42) à chacune des extrémités du tronçon de ligne (21; 25).

4. Substrat à matrice active pour un dispositif d'affichage, selon l'une quelconque des revendications 1 à 3, dans lequel lesdits tronçons de ligne de contournement de grille (22) possèdent ladite structure à deux couches.

5. Substrat à matrice active pour un dispositif d'affichage, selon l'une quelconque des revendications précédentes, dans lequel des zones d'une couche d'ITO en forme de film (57), déposée pour constituer lesdites électrodes d'élément d'image (30), couvrent l'une des couches conductrices (55) des tronçons de lignes de grille et de source.

6. Substrat à matrice active pour un dispositif d'affichage, selon l'une quelconque des revendications précédentes, dans lequel lesdits moyens de commutation comprennent deux transistors en couches minces (31, 32) connectés à la paire ligne de source/ligne de grille associée, en parallèle sur celle-ci.

Fig.1

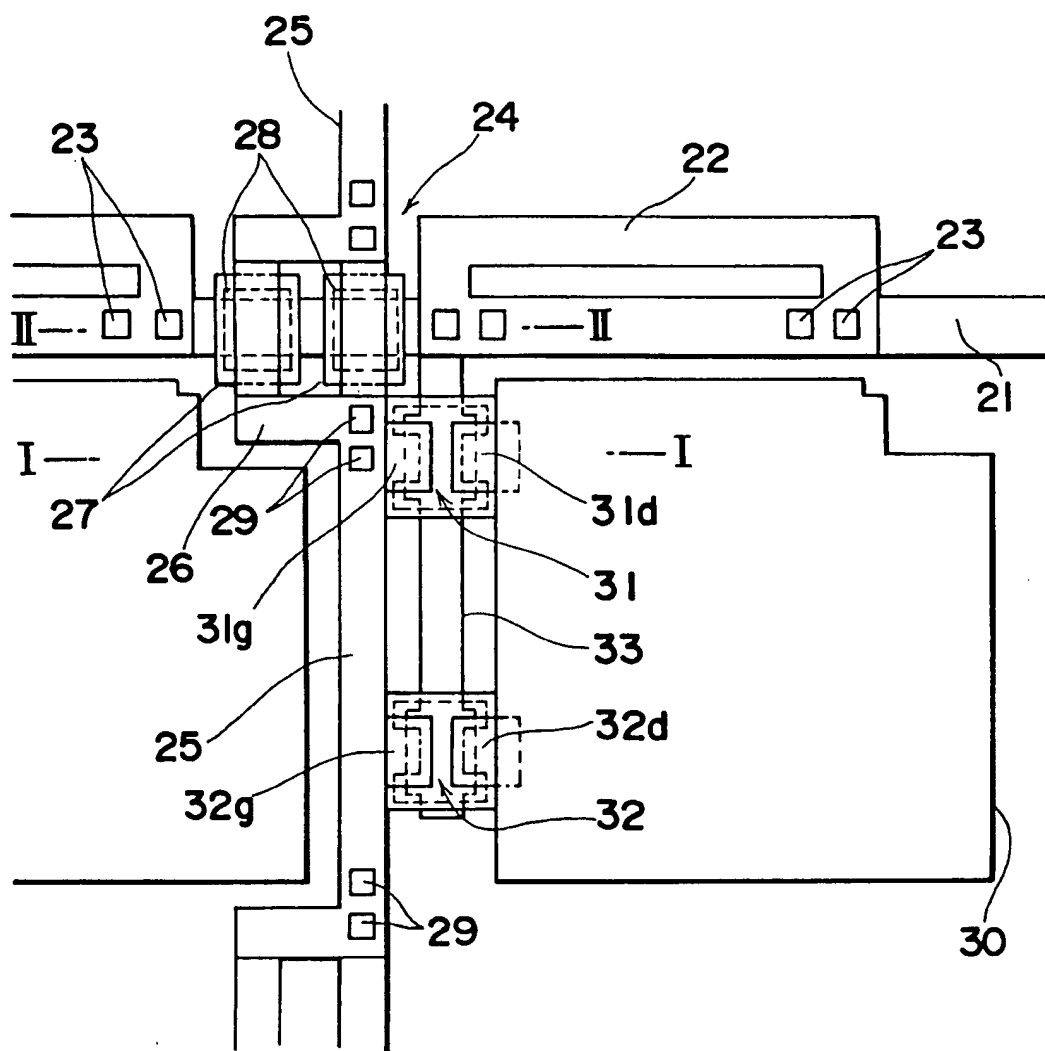


Fig.2

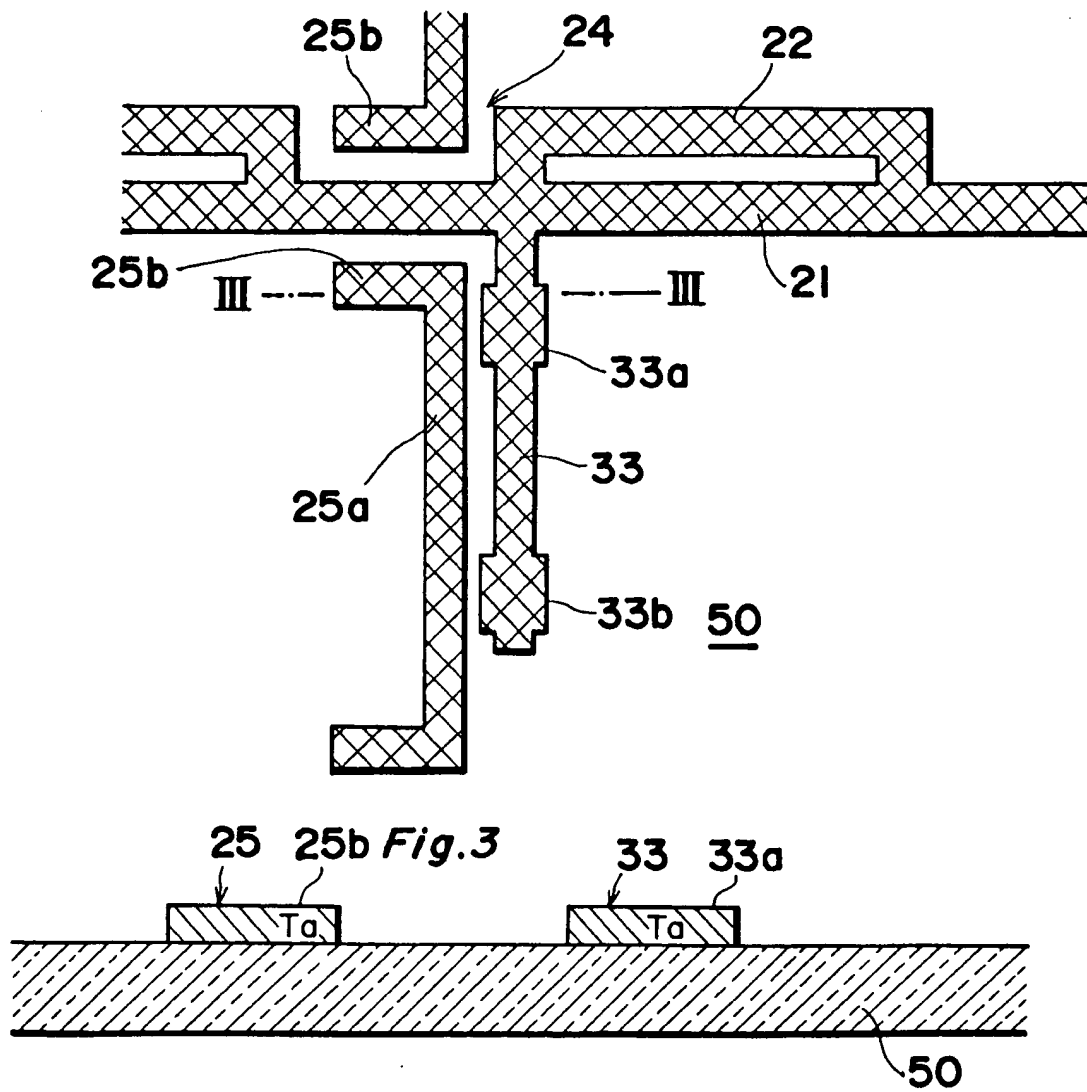


Fig. 4

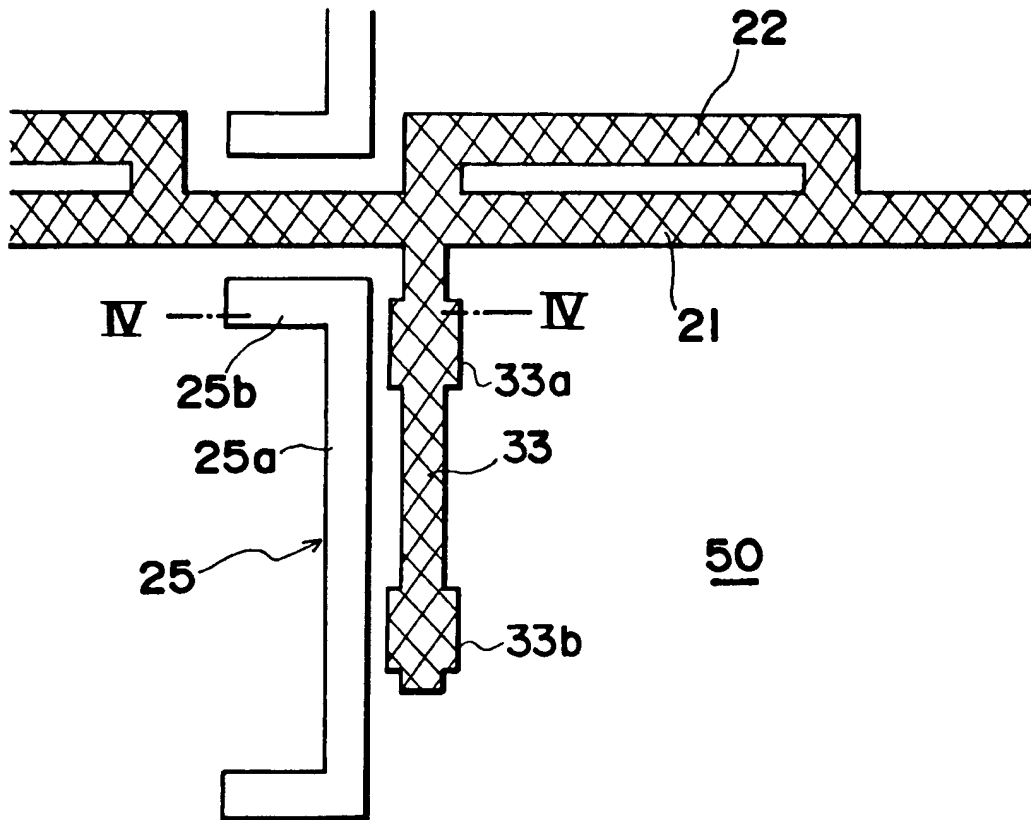


Fig. 5

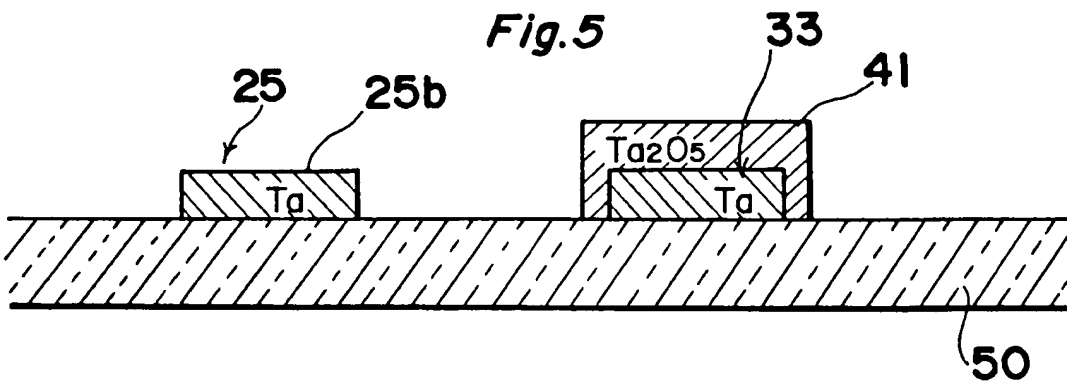


Fig.6

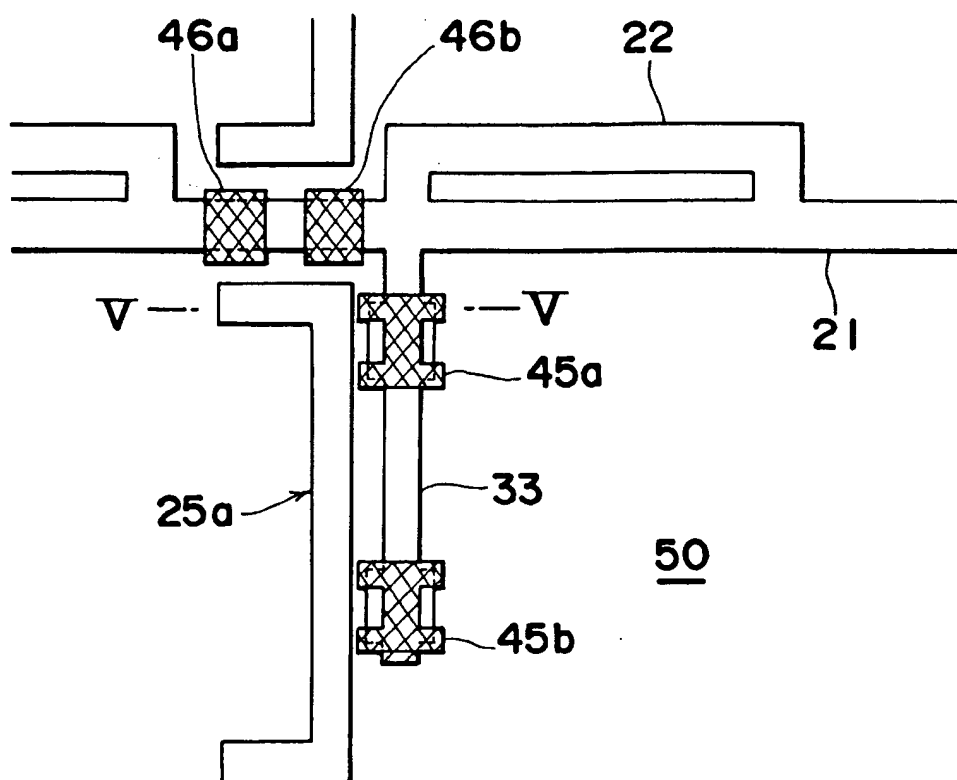


Fig.7

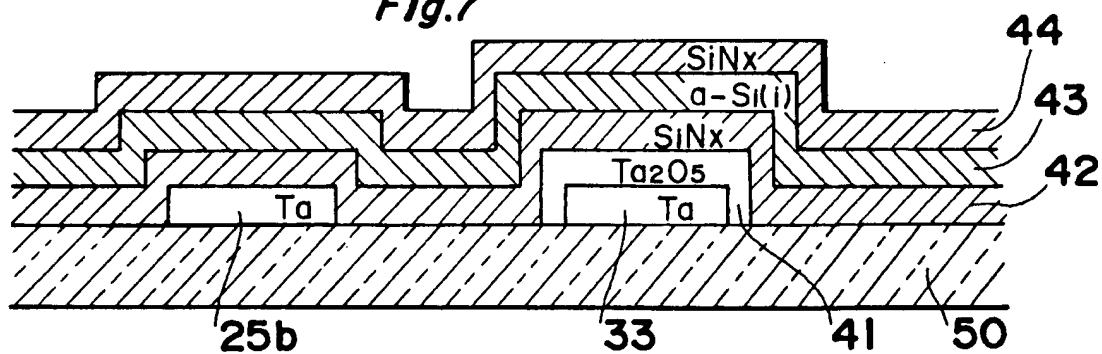


Fig.8

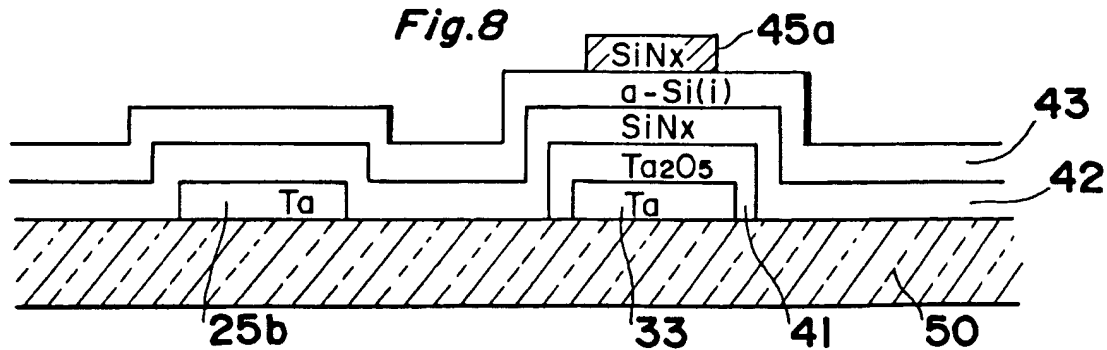


Fig.9

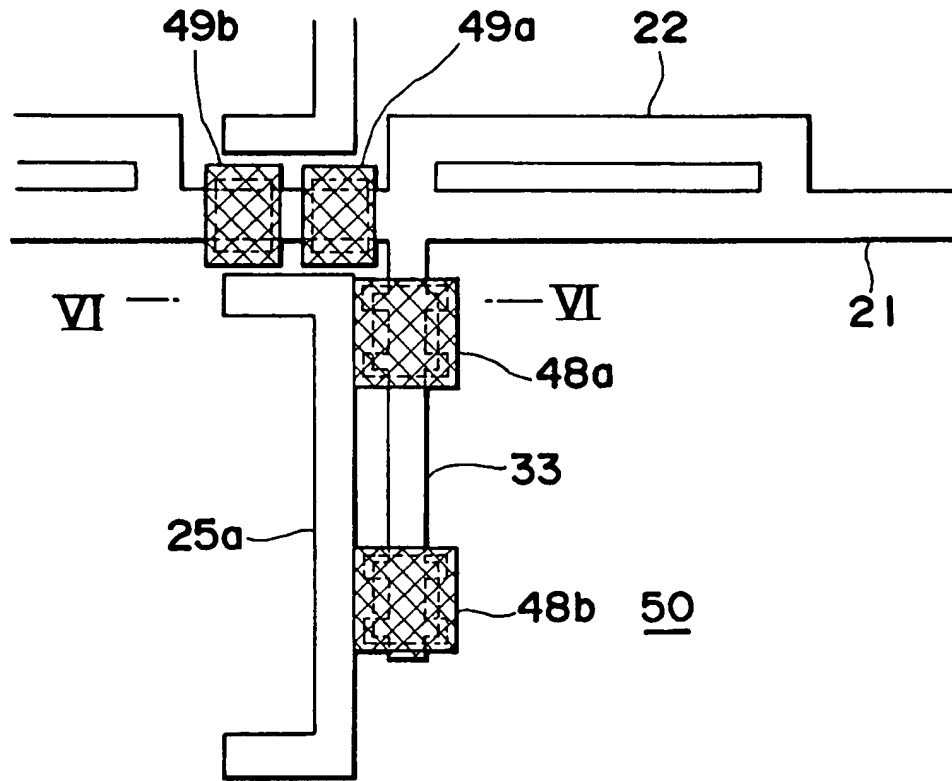


Fig.10

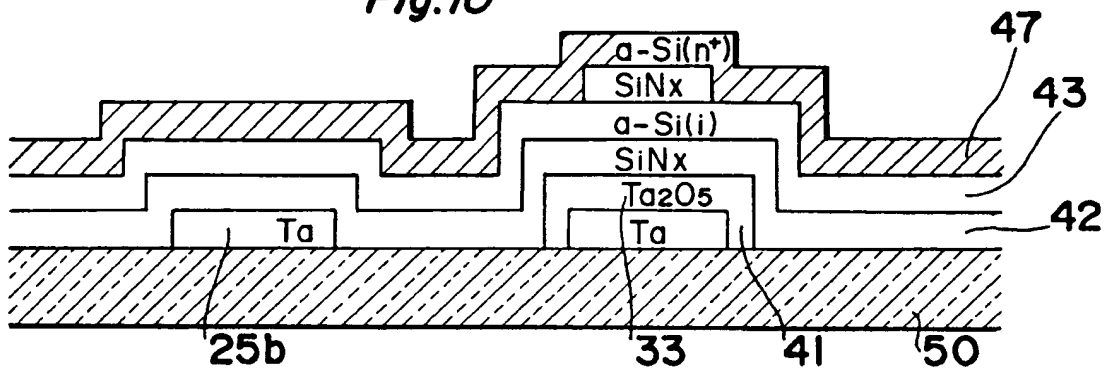


Fig.11

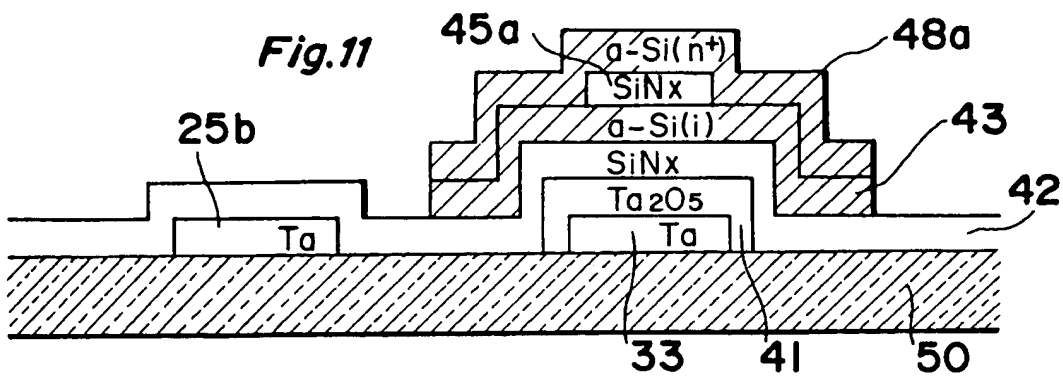


Fig.12

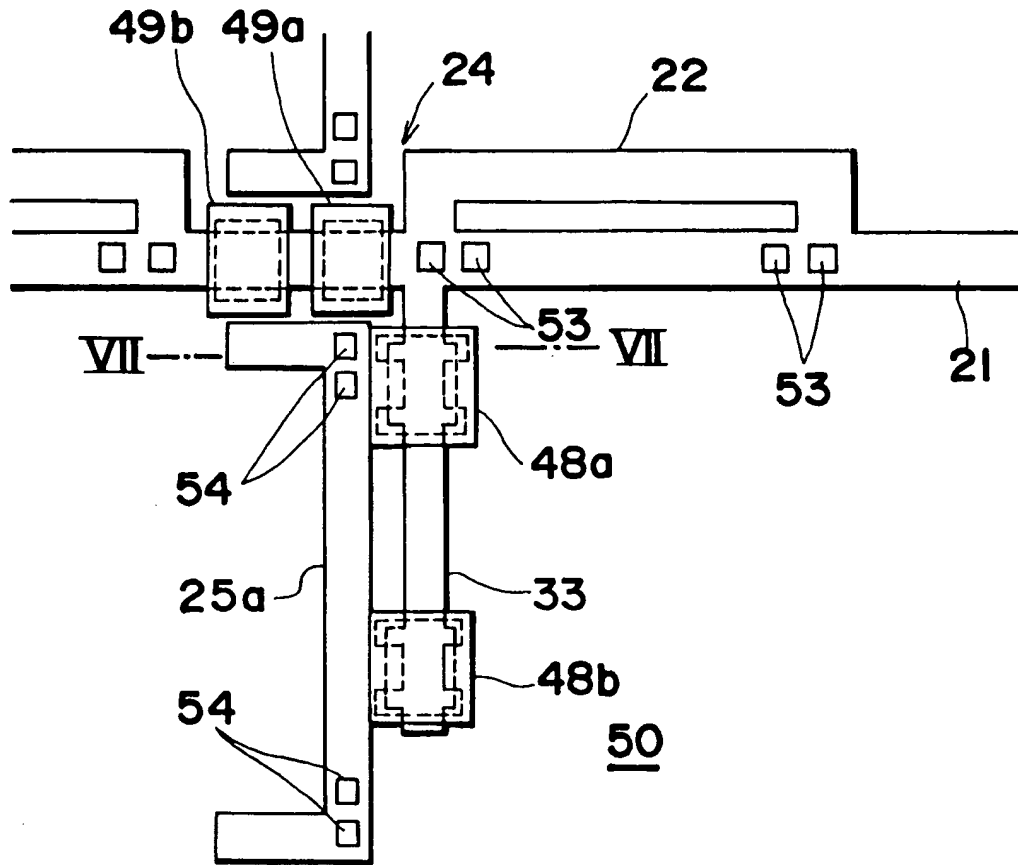


Fig.13

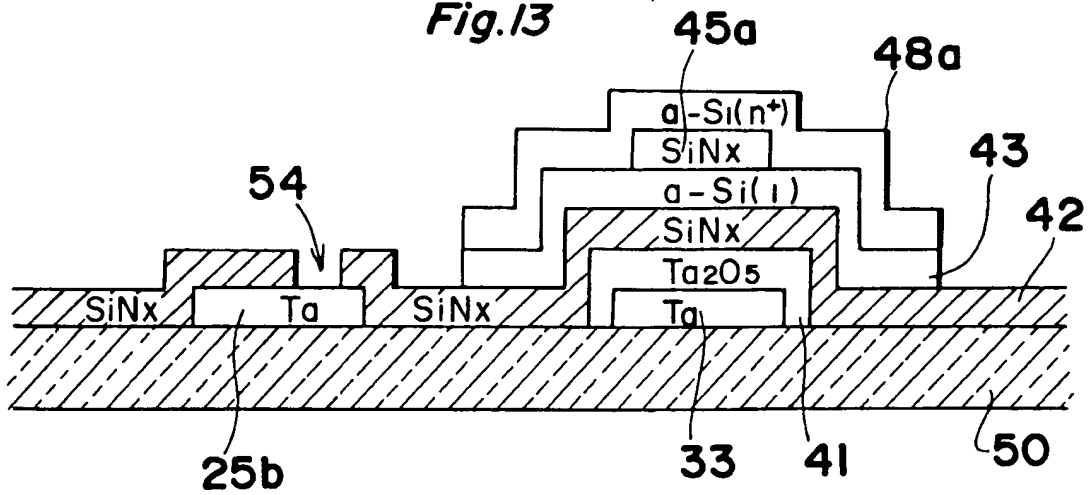


Fig. 14

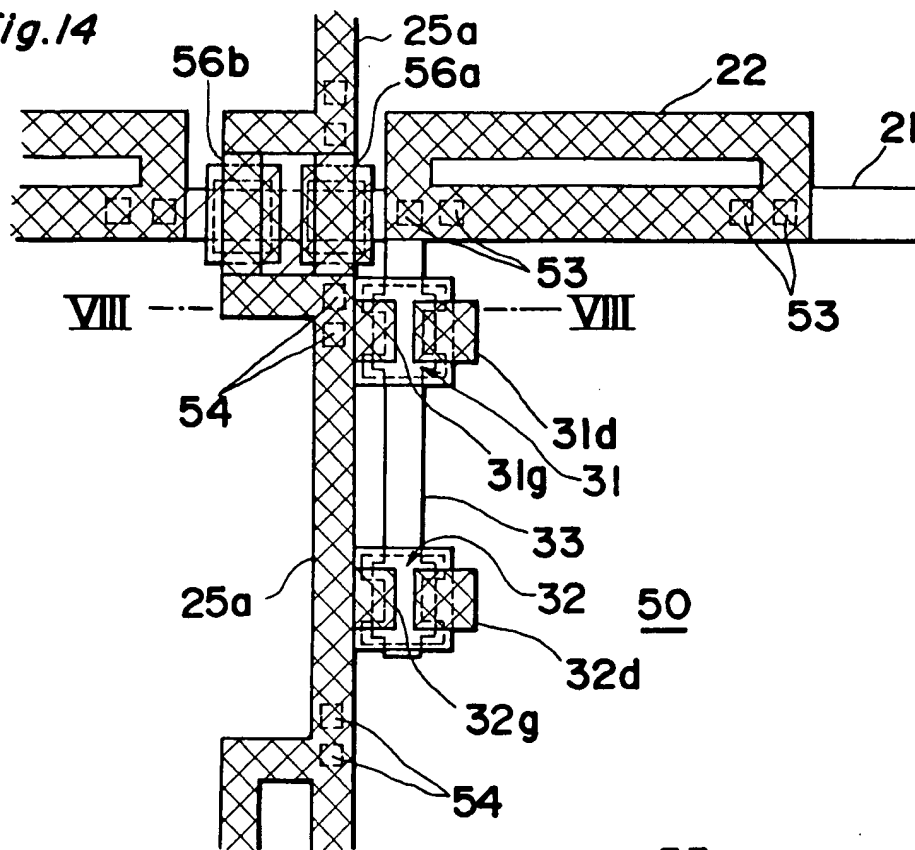


Fig. 15

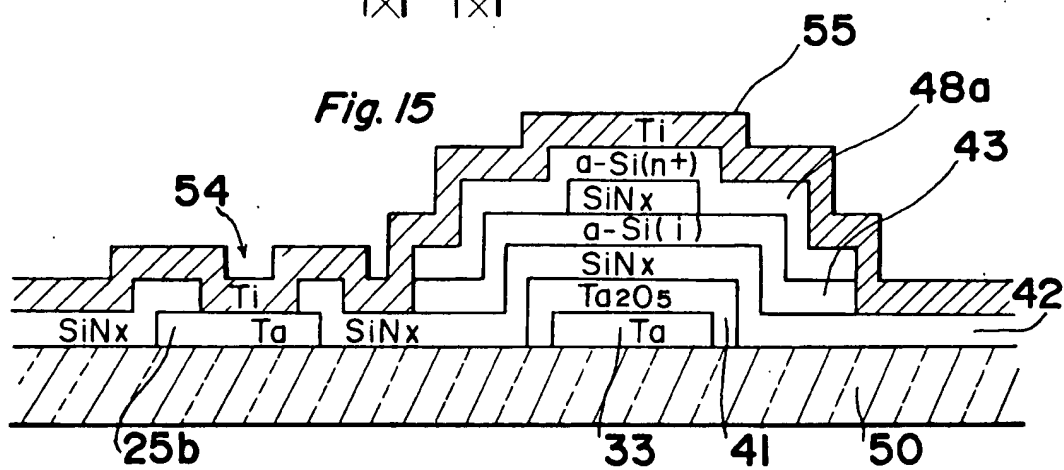
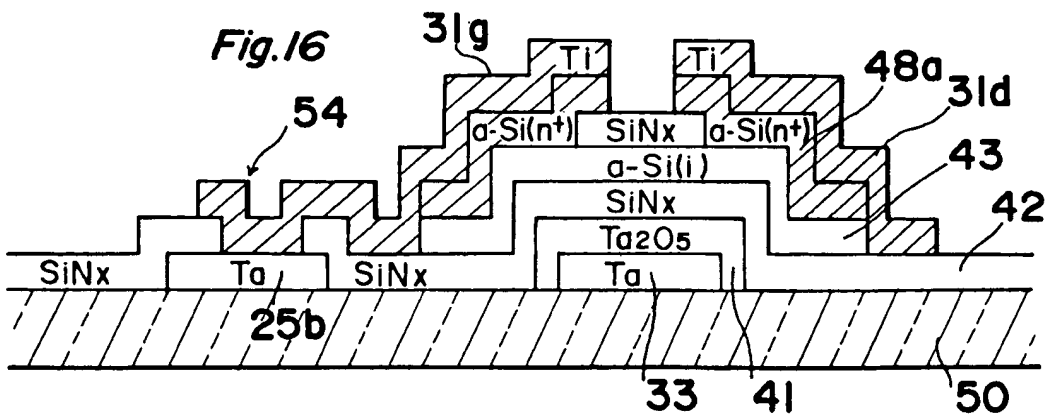


Fig. 16



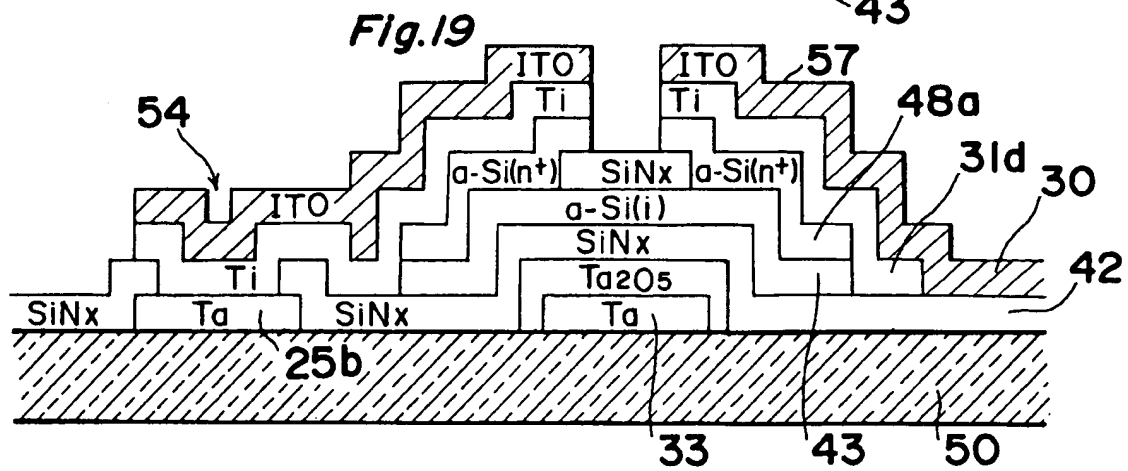
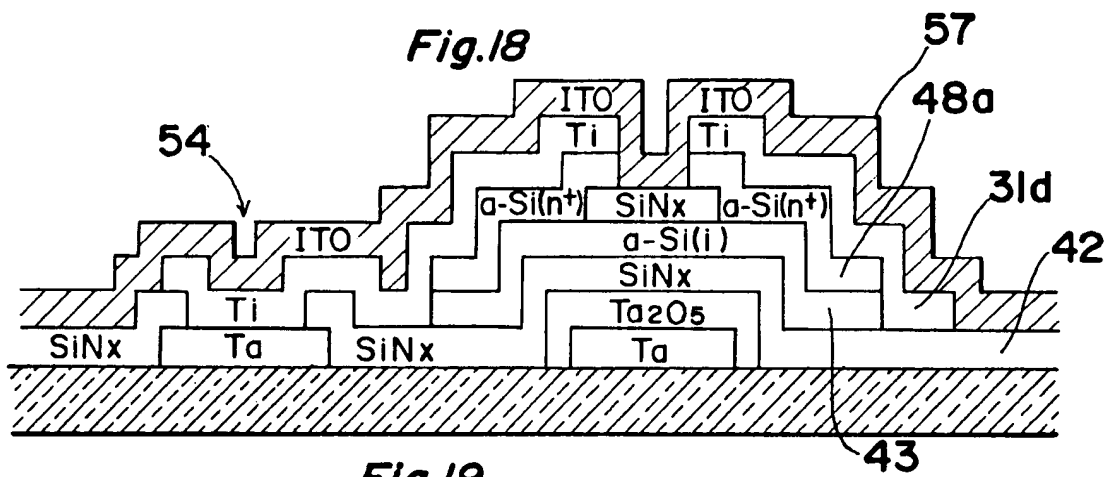
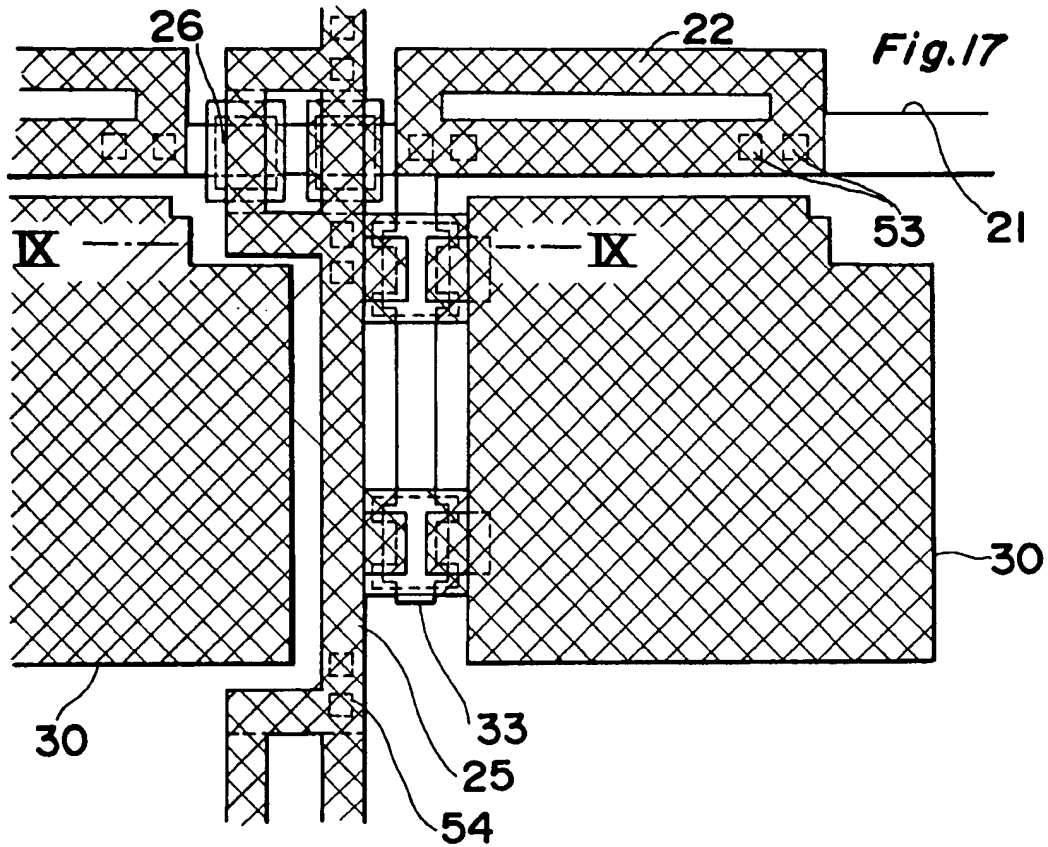


Fig. 20

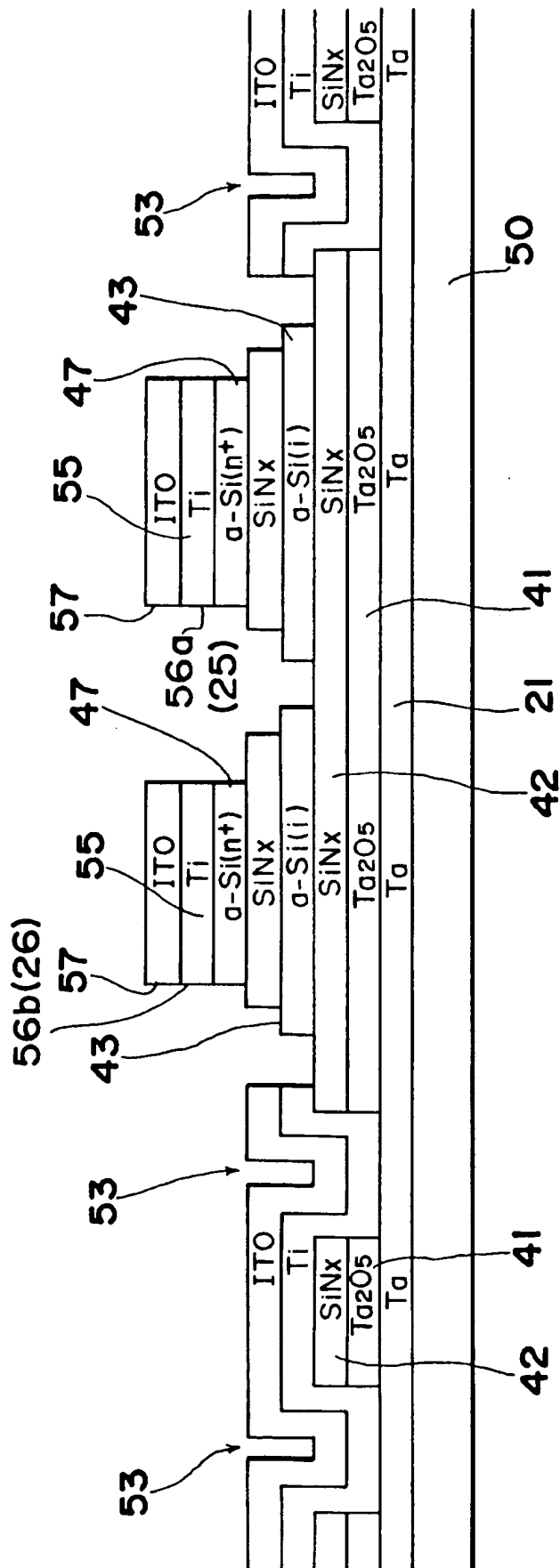


Fig. 21

	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈	Y _n
X ₁	A ₁₁	A ₁₂	A ₁₃	A ₁₄	A ₁₅	A ₁₆	A ₁₇	---	---
X ₂	A ₂₁	A ₂₂	A ₂₃	A ₂₄	A ₂₅	A ₂₆	A ₂₇	---	A _{1n}
X ₃	A ₃₁	A ₃₂	A ₃₃	A ₃₄	A ₃₅	A ₃₆	A ₃₇	---	A _{2n}
X ₄	A ₄₁	A ₄₂	A ₄₃	A ₄₄	A ₄₅	A ₄₆	A ₄₇	---	A _{3n}
X ₅	A ₅₁	A ₅₂	A ₅₃	A ₅₄	A ₅₅	A ₅₆	A ₅₇	---	A _{4n}
X ₆	A ₆₁	A ₆₂	A ₆₃	A ₆₄	A ₆₅	A ₆₆	A ₆₇	---	A _{5n}
X ₇	A ₇₁	A ₇₂	A ₇₃	A ₇₄	A ₇₅	A ₇₆	A ₇₇	---	A _{6n}
X ₈	---	---	---	---	---	---	---	---	A _{7n}
---	---	---	---	---	---	---	---	---	---
X _m	A _{m1}	A _{m2}	A _{m3}	A _{m4}	A _{m5}	A _{m6}	A _{m7}	---	A _{mn}

Fig. 22

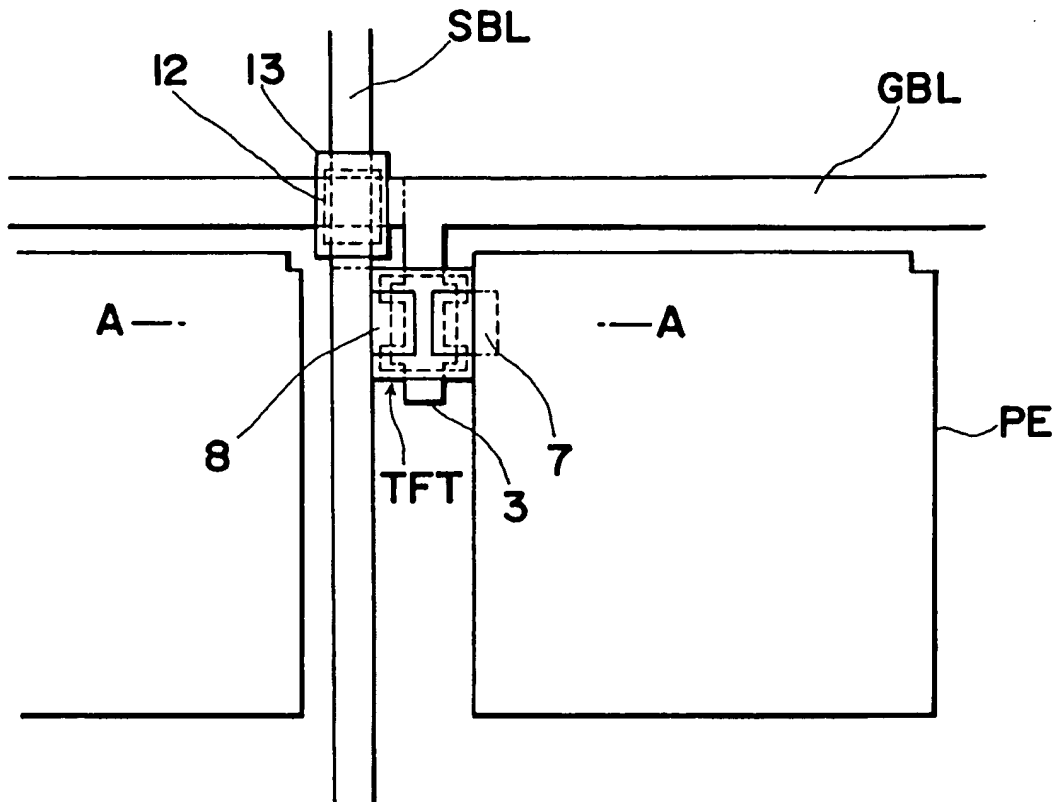


Fig. 23

